DesignCon 2012

WHERE CHIPHEADS CONNECT

Simulating Large Systems with Thousands of Serial Links

Session 8-WA3

UBM Electronics

DesignCon 2012

WHERE CHIPHEADS CONNECT

About the Authors

Donald Telian is an independent Signal Integrity Consultant. Building on over 25 years of SI experience at Intel, Cadence, HP, and others, his recent focus has been on helping customers correctly implement today's Multi-Gigabit serial links. He has published numerous works on this and other topics that are available at his website siguys.com. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries.

Sergio Camerlo is an Engineering Director with Ericsson Silicon Valley (ESV), which he joined through the Redback Networks acquisition. His responsibilities include the Chassis/Backplane infrastructure design, PCB Layout Design, System and Board Power Design, Signal and Power Integrity. He also serves on the company Patent Committee and is a member of the ESV Systems and Technologies HW Technical Council. In his previous assignment, Sergio was VP, Systems Engineering at MetaRAM, a local startup, where he dealt with die stacking and 3D integration of memory. Before, Sergio spent close to a decade at Cisco Systems, where he served in different management capacities. Sergio has been awarded fourteen U.S. Patents on signal and power distribution, interconnects and packaging.

Barry Katz, President and CTO for SiSoft, founded SiSoft in 1995. As CTO, Barry is responsible for leading the definition and development of SiSoft's products. He has devoted much of his efforts at SiSoft to delivering a comprehensive design methodology, software tools, and expert consulting to solve the problems faced by designers of leading edge high-speed systems. He was the founding chairman of the IBIS Quality committee. Barry received an MSEE degree from Carnegie Mellon and a BSEE degree from the University of Florida.

Dr. Walter Katz, Chief Scientist for SiSoft, is a pioneer in the development of constraint driven printed circuit board routers. He developed SciCards, the first commercially successful auto-router. Dr. Katz founded Layout Concepts and sold routers through Cadence, Zuken, Daisix, Intergraph and Accel. More than 20,000 copies of his tools have been used worldwide. Dr. Katz developed the first signal integrity tools for a 17 MHz 32-bit minicomputer in the seventies. In 1991, IBM used his software to design a 1 GHz computer. Dr. Katz holds a PhD from the University of Rochester, a BS from Polytechnic Institute of Brooklyn and has been awarded 5 U.S. Patents.

Michael Steinberger, Ph.D., Lead Architect for SiSoft, has over 30 years experience designing very high speed electronic circuits. Dr. Steinberger holds a Ph.D. from the University of Southern California and has been awarded 14 patents. He is currently responsible for the architecture of SiSoft's Quantum Channel Designer tool for high speed serial channel analysis. Before joining SiSoft, Dr. Steinberger led a group at Cray, Inc. performing SerDes design, high speed channel analysis, PCB design and custom RAM design.

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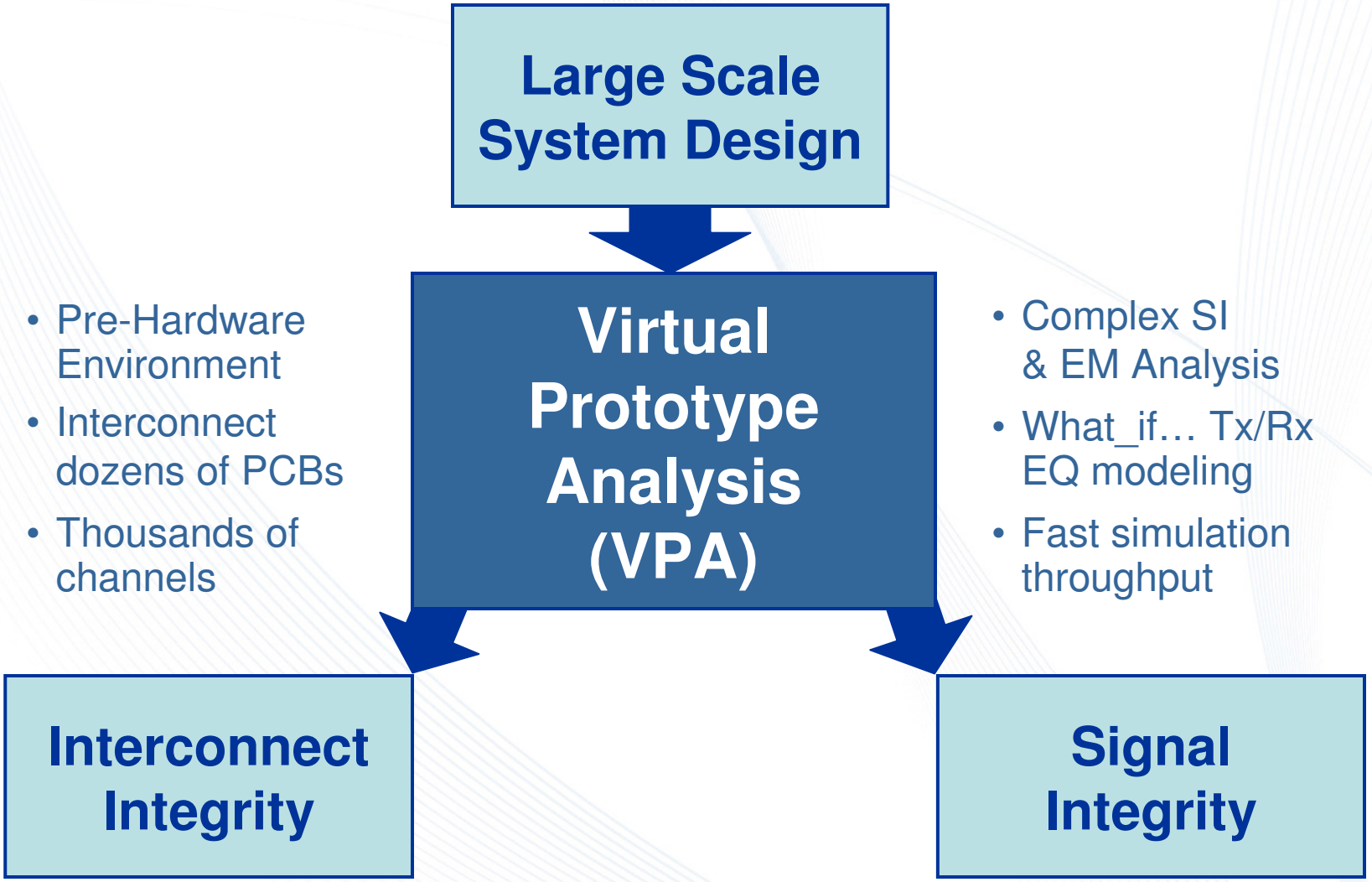
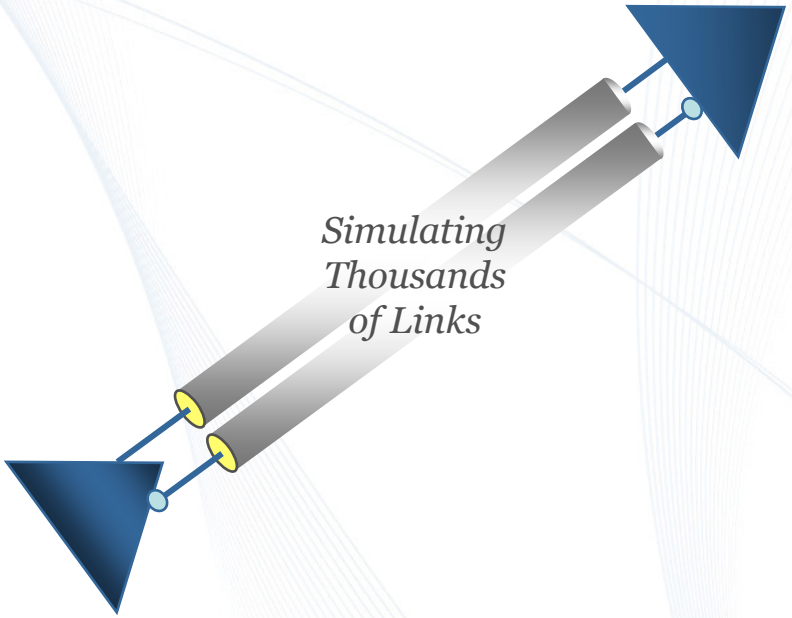
Design Process



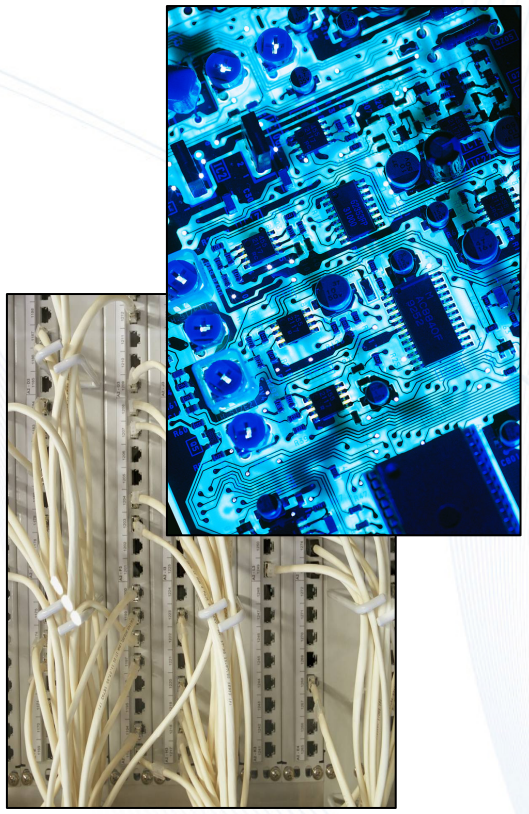
Agenda

- Virtual Prototype Analysis
  - Example system
  - Connectivity check
  - Quantify design margin
  - Isolate resonances
  - Balance system EQ
  - Guide design choices
- Technology Enablers
  - Post-equalized Rx eye
  - Fast & accurate via models
  - Capacity, throughput, data mining



Example System

- 30 Large-scale PCBs
  - Over 7k square inches of PCB
- 50+ layer backplane
  - Dozens of connectors
- Thousands of serial links
  - Ranging 12” to 36” long

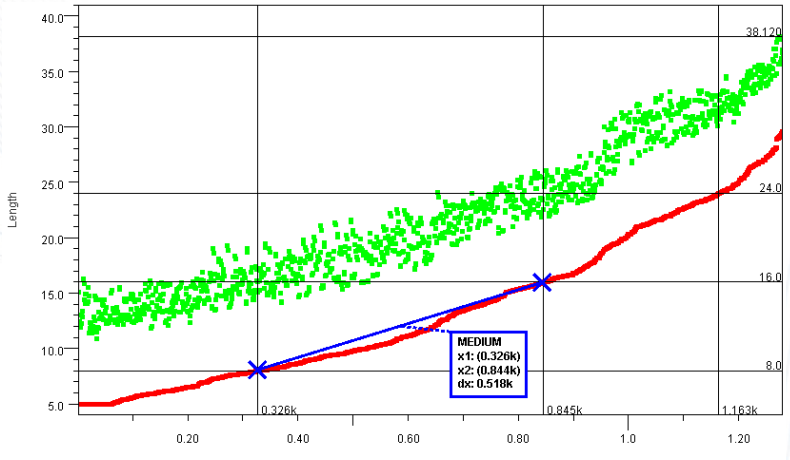


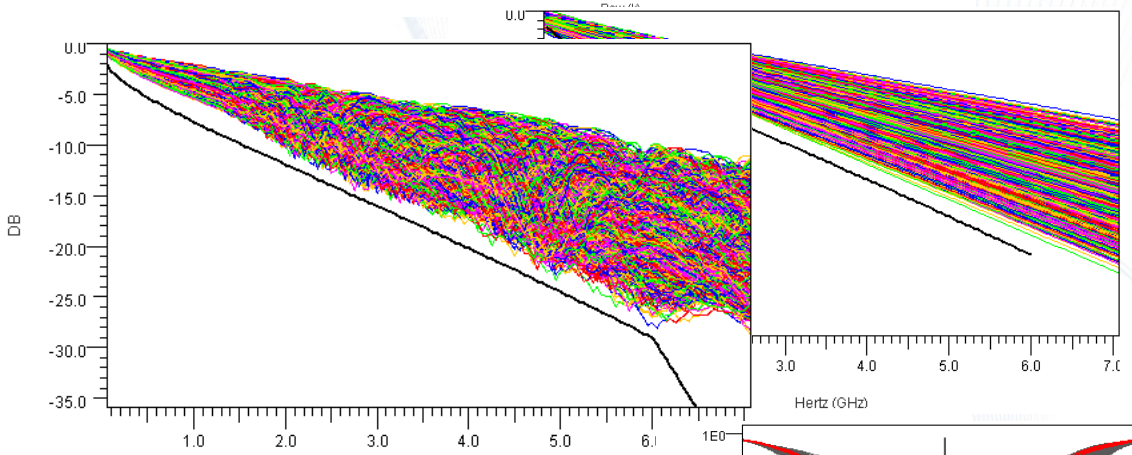
Connectivity Check

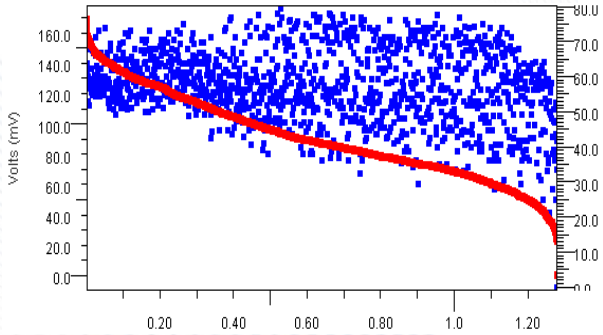
- Confirm system-level “Interconnect Integrity”
- Test-bench for new/revised PCBs
- Leverages prep for simulation
- Gate to new PCB fabout

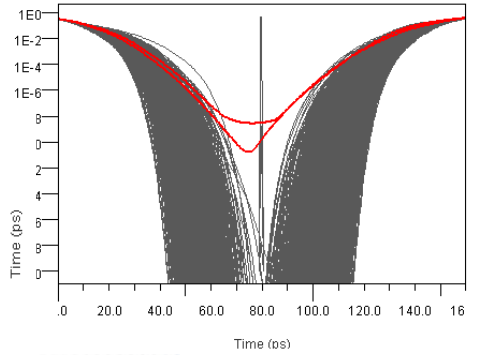
Connectivity

- Physical
- Electrical
- Operational



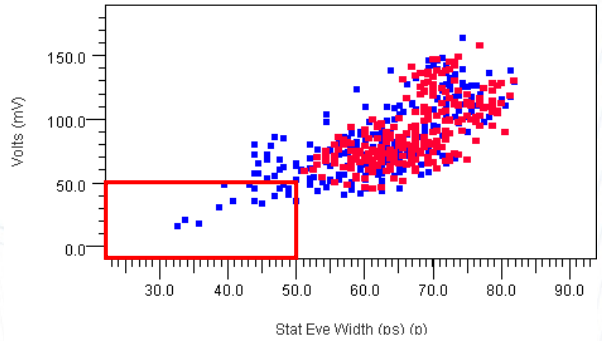


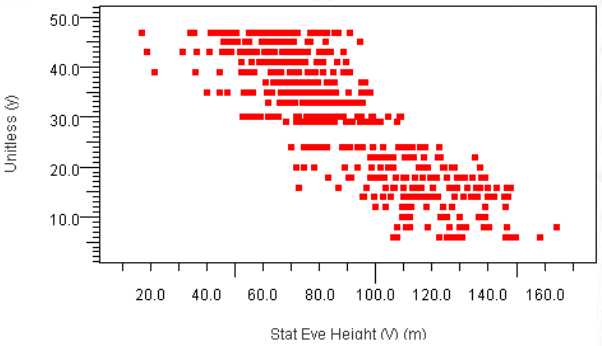


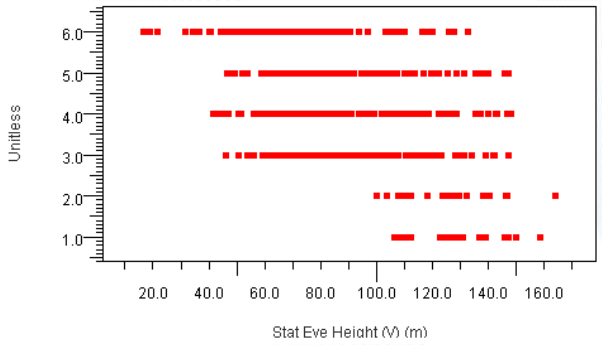


Design Margin

- Eye Height vs Width
  - Red = A -> B
  - Blue = B -> A
- Eye Height vs BP Layer
  - Deeper layers ~= decreasing height
- Height vs Connector Row
  - Worst heights on higher# rows

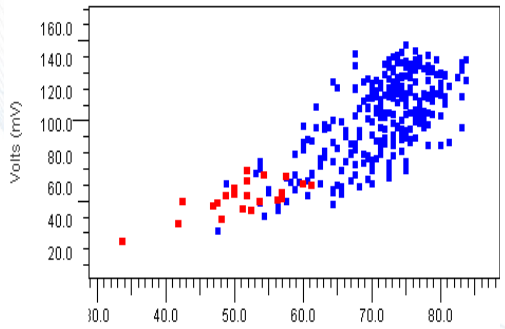




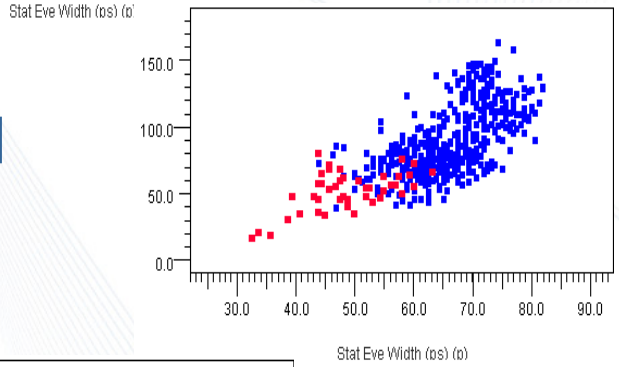


Filter And Scale

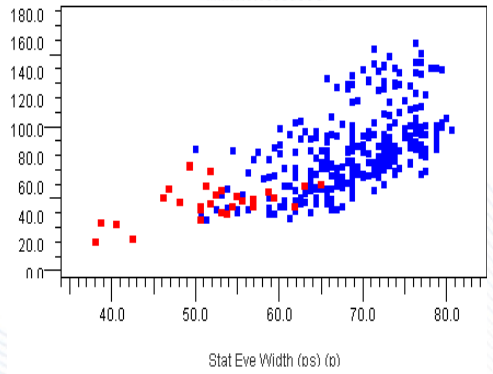
- Filter (red) =
  - B -> A, and
  - Deep BP layer, and
  - Connector row 6
- Short, Med, Long
  - ~12”, 24”, 36”
- Same performance limiter across range of channel lengths



Short

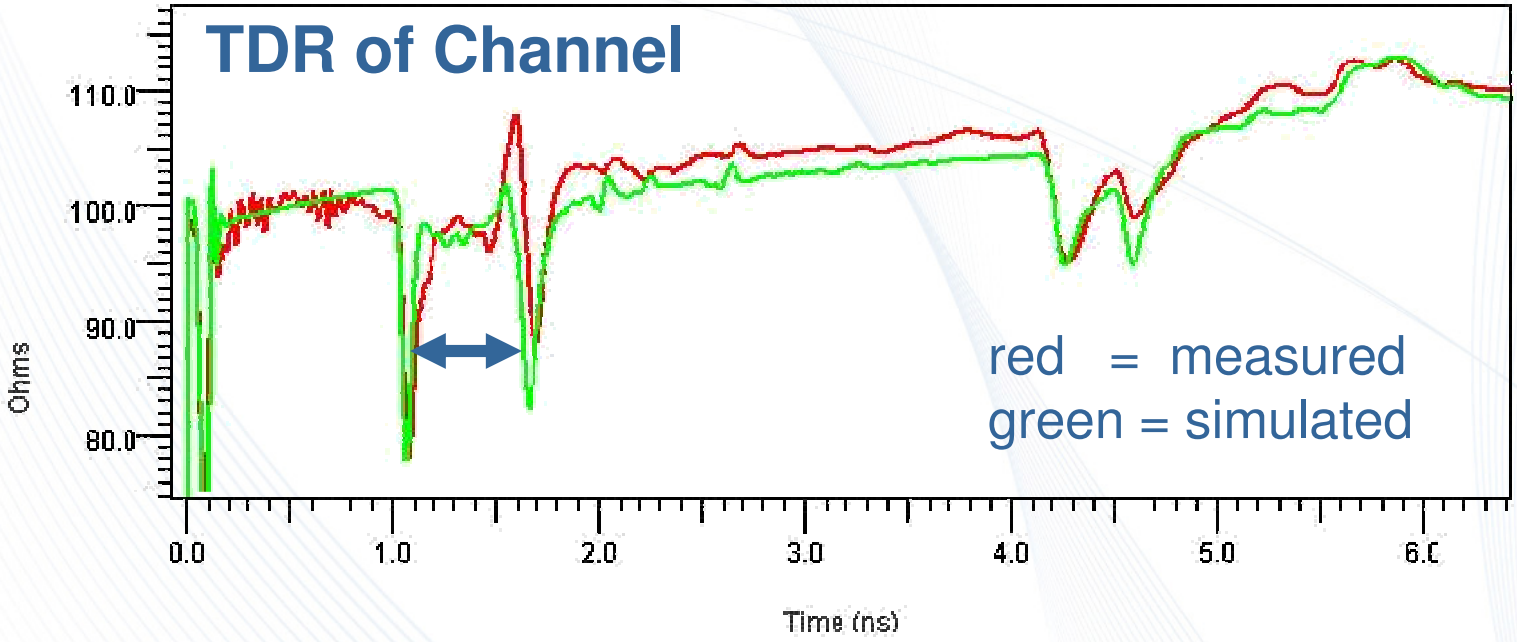


Med



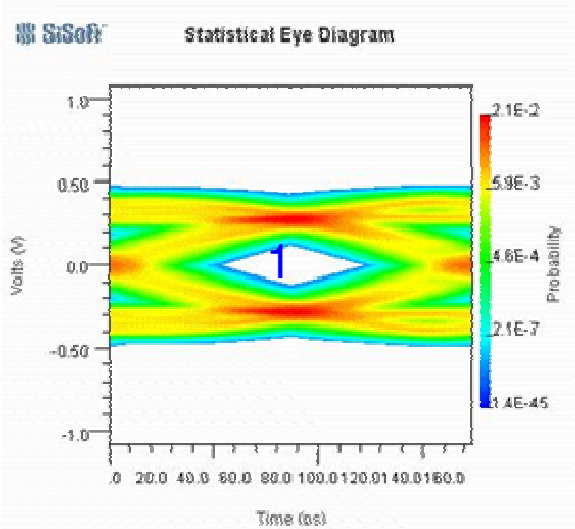
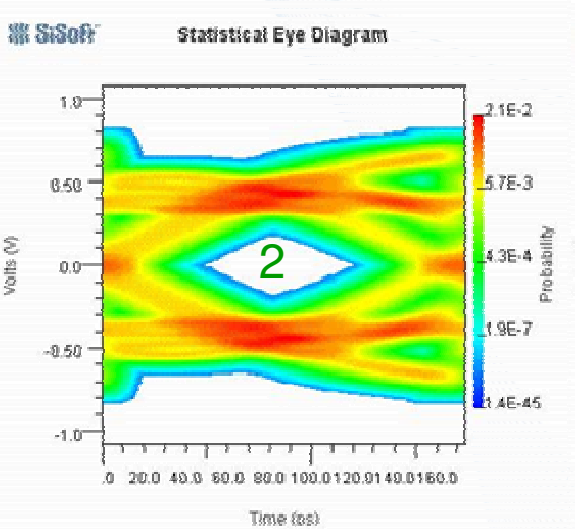
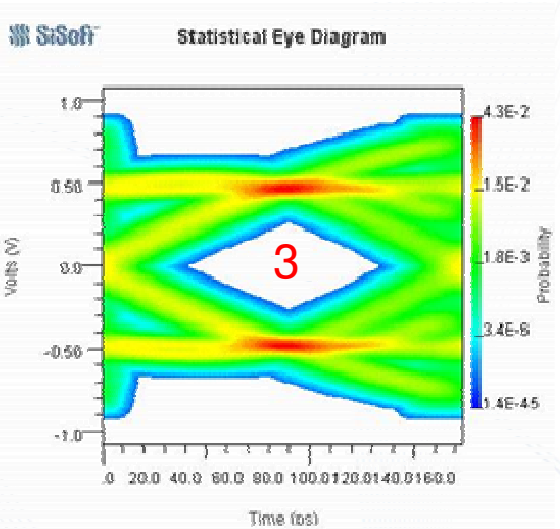
Long

Discontinuity Induced Resonance



- Standing waves between connector vias
- 1/roundtrip ~= 1.5 GHz
- Reduces 6 Gbps design margin

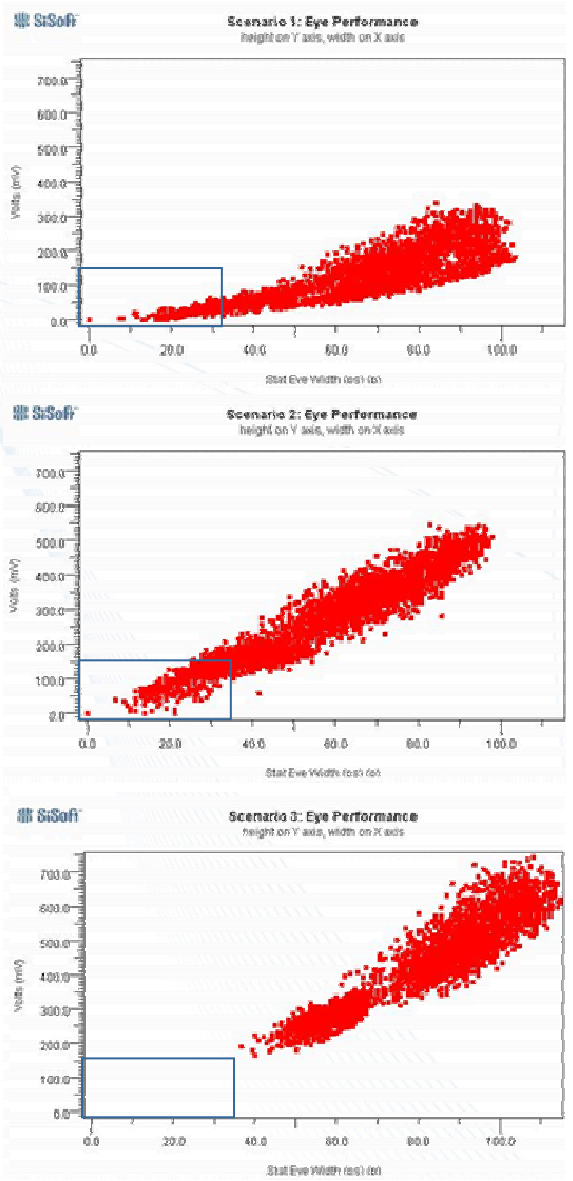
Balancing System-level EQ

Post:	Tx=-35%, Rx=-2%	Tx=-17%, Rx=-18%	Tx=0%, Rx=-32%
			
Eye:	248mV / 72pS	345mV / 73pS	513mV / 94pS

- Pre-cursor=Tx, Post-cursor=(Rx and/or Tx)??
- Trade Post, measure at output of Rx EQ
- 100% height increase, 30% width increase at Rx out

Three EQ Options: Thousands of Links

- Over 20,000 simulations
- Processed to 10^{-12} probability
- 3 seconds per simulation
  - 4 hours on 8 CPUs



1

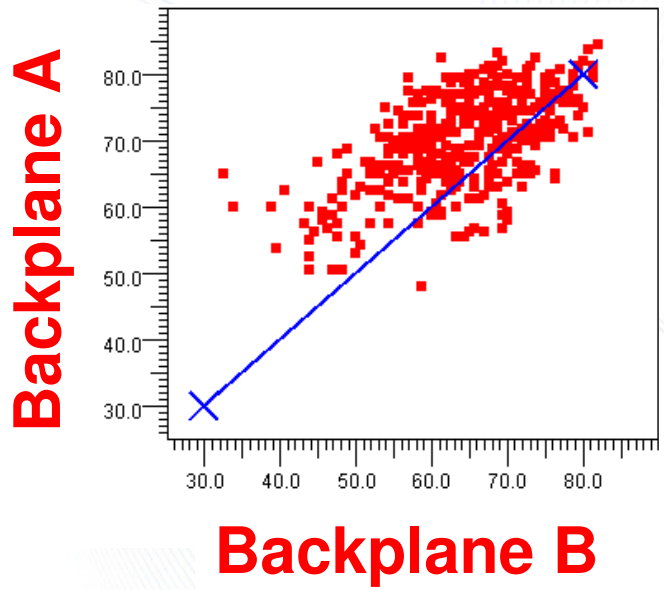
2

3

Guide Design Choices

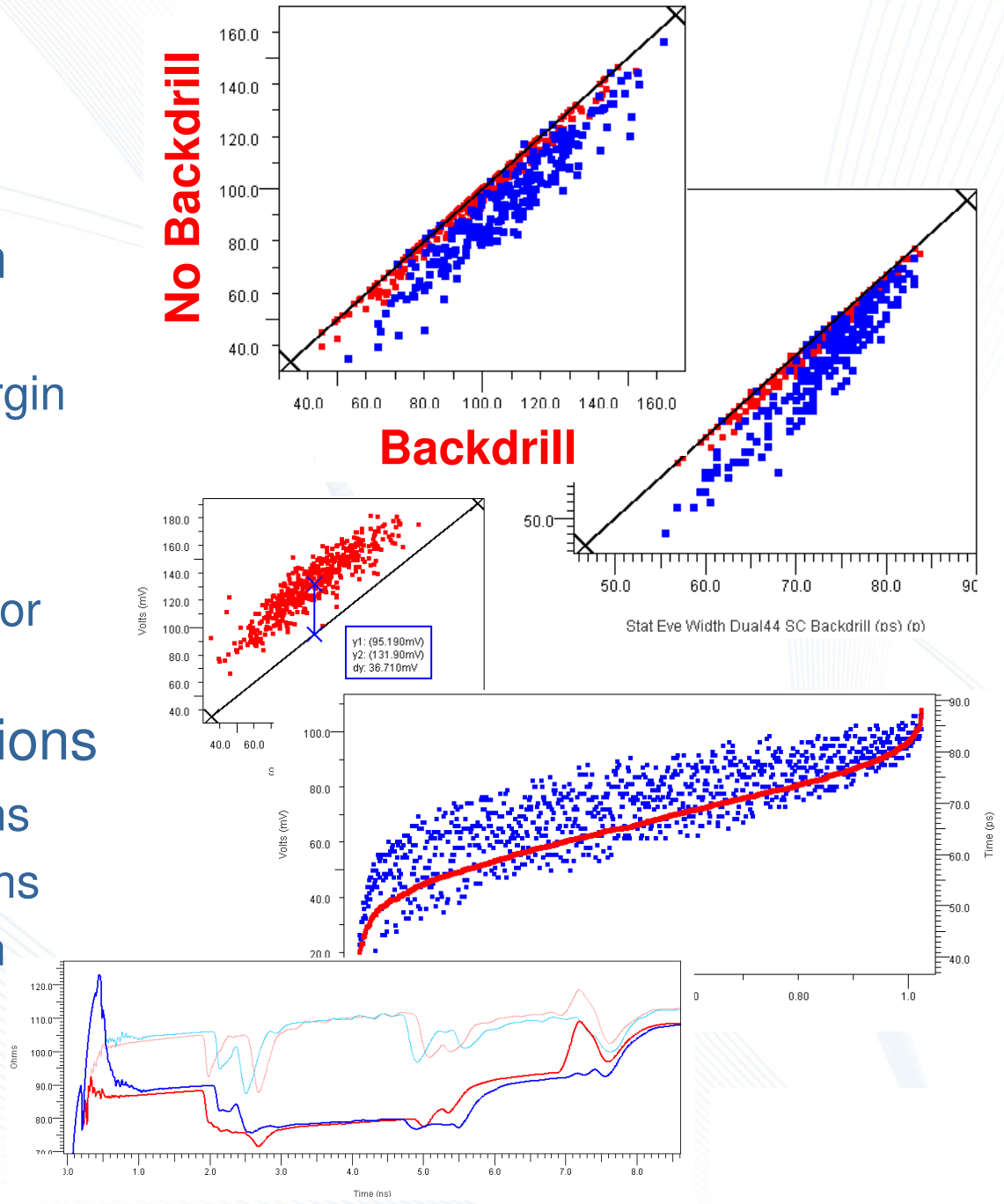
VPA examines options that require too much time and expense to test in hardware, such as

- Data rate
- Alternate PCBs
- Via back-drilling
- PCB layer swaps
- Complex via structures
- Back-drill stub length (#depths)
- Length variations and constraints
- Connector/route impedance variations



VPA Design

- Back-drilling on plug-in card?
  - 20% more margin
  - Ideal increase
- Data rate
  - +30% margin for -8% reduction
- Impedance options
  - All PCBs/Conns
  - 2^{10} permutations
  - 300% variation



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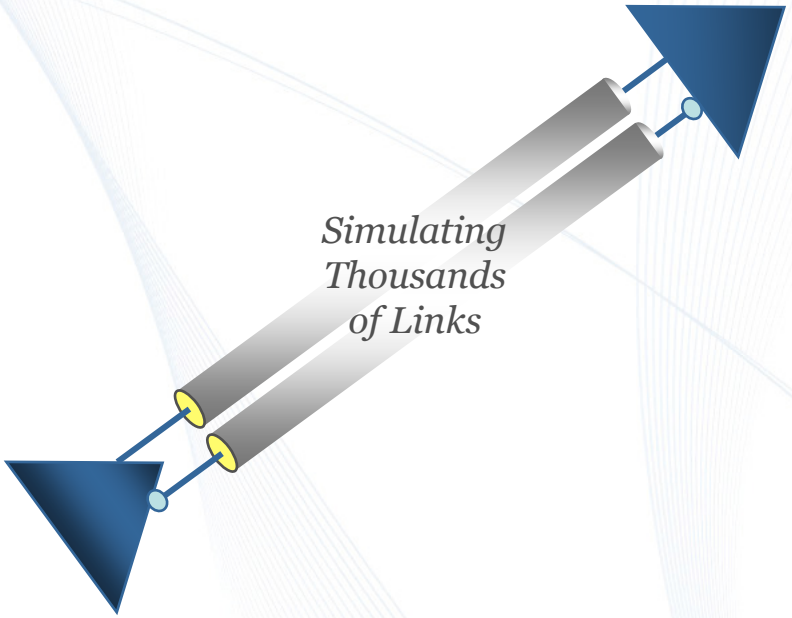
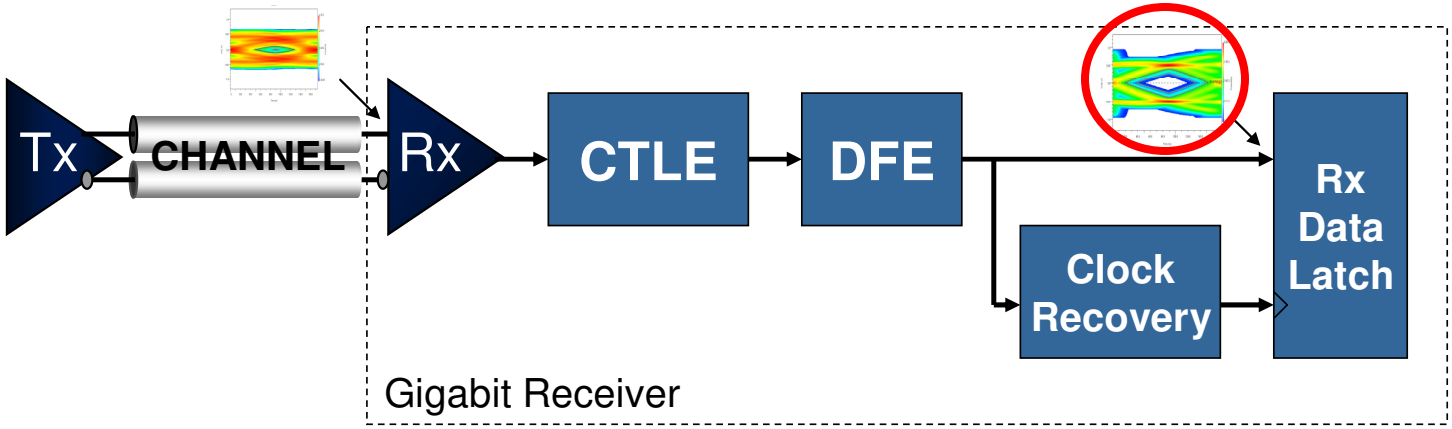


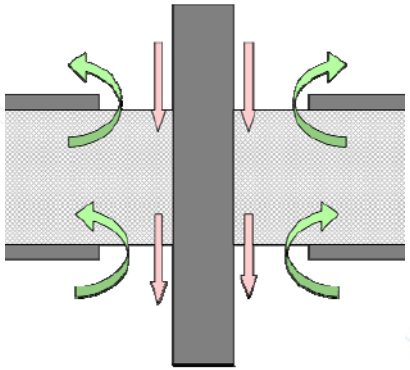
Post-equalized Rx Eye

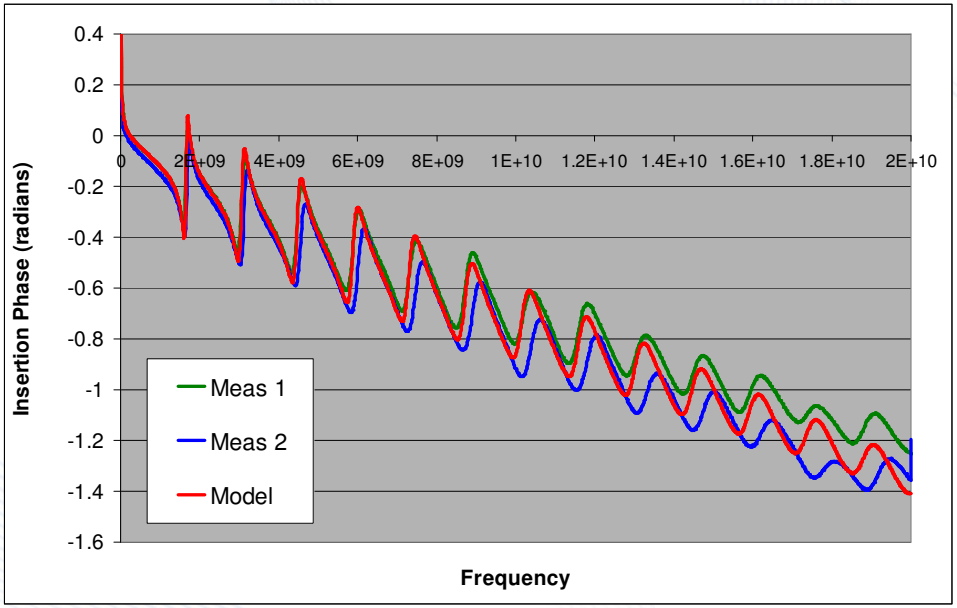


- Increasingly the only measurable Rx eye
  - And hence, signal specified by higher speed standards
- SI methodology shift – not observable on PCB
  - Measurement point often referred to as “Rx Latch”
- Adds complexity to Rx (AMI) models
  - And forces T&M equipment to add “simulation”

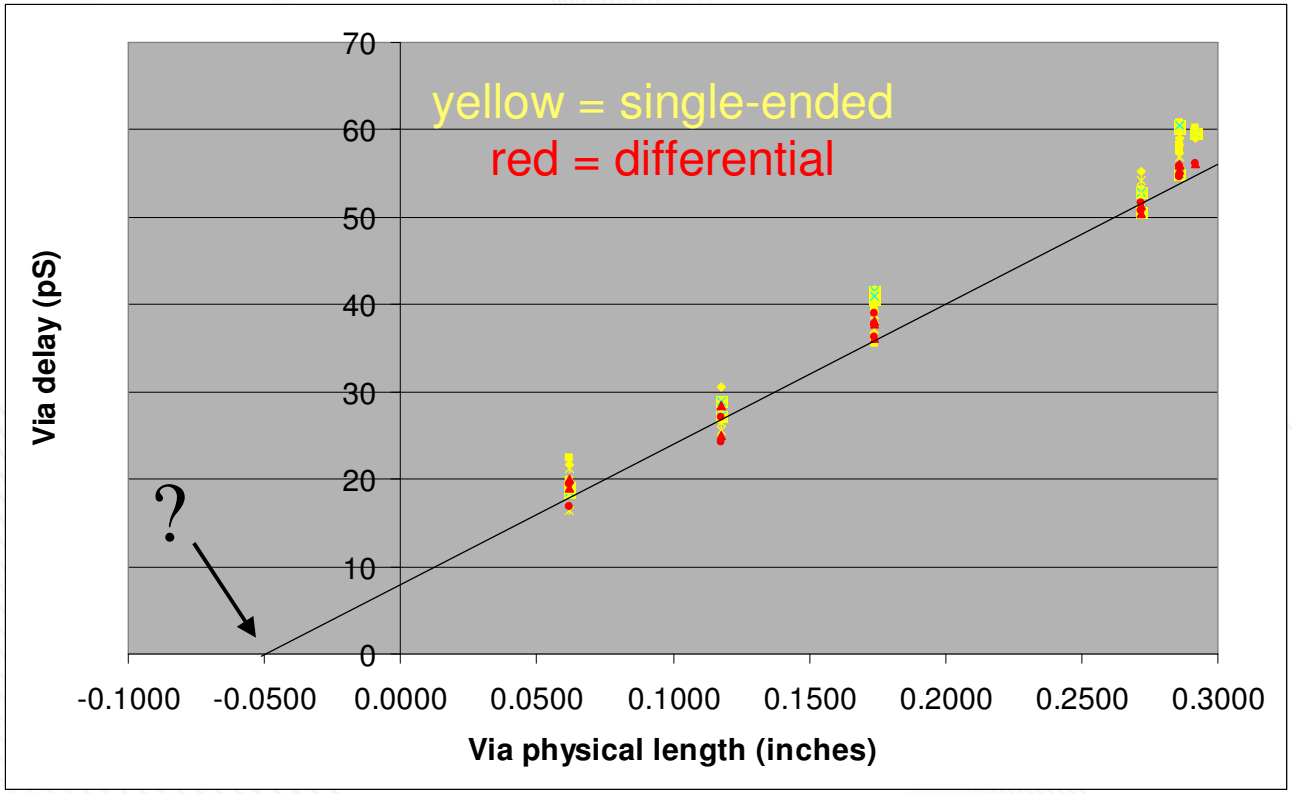
VPA Via Requirements

- Accurate via modeling critical
- Via model solution must
  - Accommodate a variety of geometries
  - Solve and simulate quickly
  - Correlate to measured data
- Various simplified via models exist
  - Typically transmission line based
  - Anisotropic or isotropic dielectric?





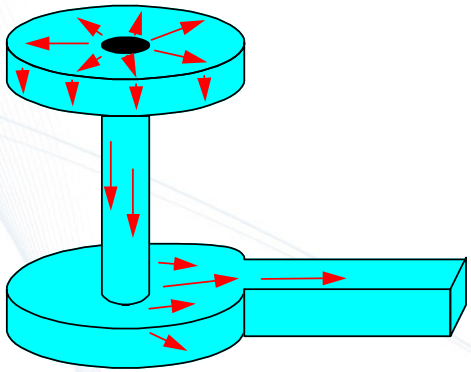
Via Measurements

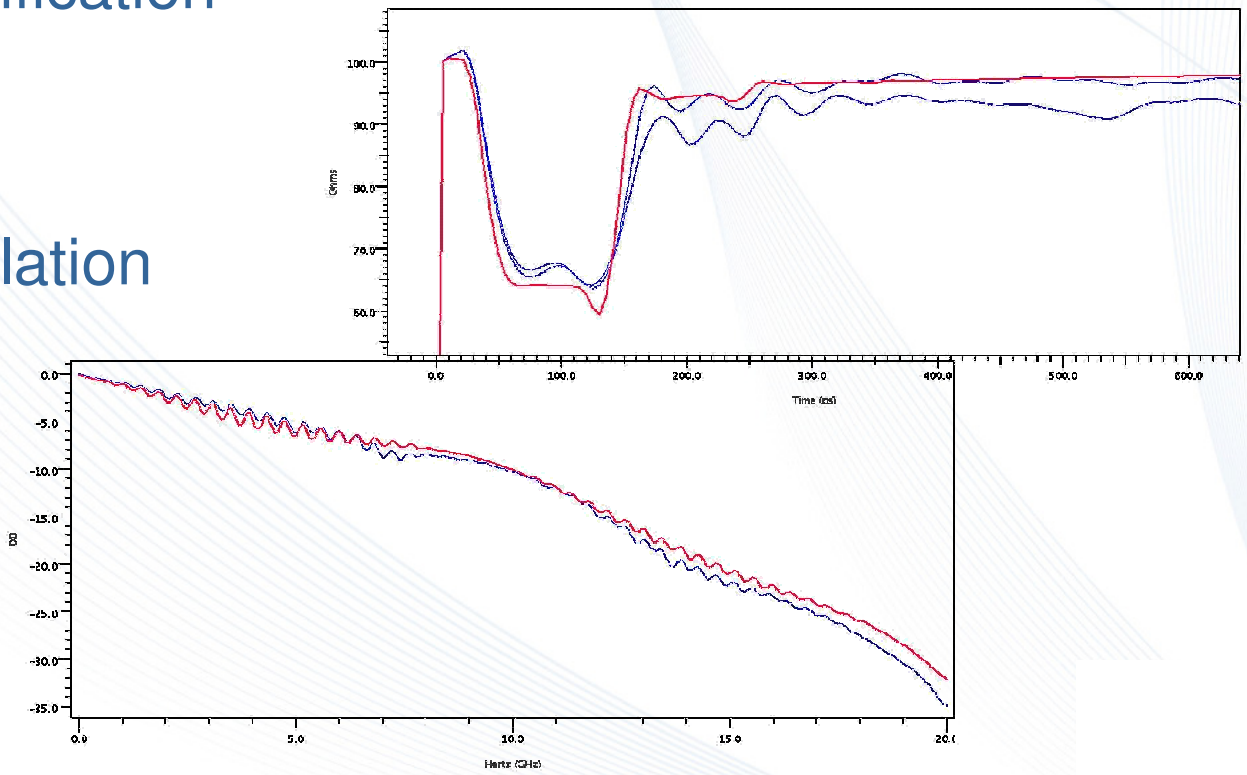


- High-precision TDR from measured S Parameters
- Electrical length /= physical length ?
- Hypothesis: include length around pad

Adapted Model / Correlation

- Surface current
- Simplification
- Correlation



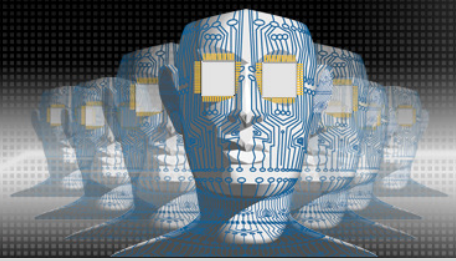


VPA Environment Requirements

- **Capacity**
  - 10s of PCBs, 250,000 Nets, millions of pins
- **Throughput**
  - 48 hour prepare, process, propose turnaround time
  - Fast extraction/simulation of all relevant structures
- **Data Mining**
  - Plot anything versus anything
  - Automated reporting
    - Physical, electrical, compliance, metrics, sorting
  - Interactive drill-down
    - Probe any location, apply masks, modify/re-simulate

Summary

- Serial Scaling: Frequency and Width
  - Frequency: new structures and EQ to model
  - Width: simulation and data processing challenge
- Parallelization of Serial Interfaces
- Virtual Prototype Analysis
  - Connectivity, design margin
  - Resonances, EQ balancing
  - Guide design choices
- The system is the model



Questions

THANK YOU

SI GUYS

ERICSSON

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