DesignCon 2012

WHERE CHIPHEADS CONNECT

Channel Eye Diagram Generation, Pre-Hardware

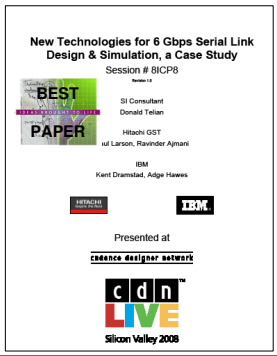
Tutorial 2-MP2, Session 3

UBM Electronics

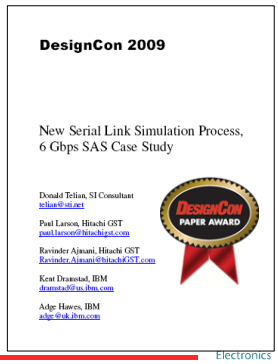
DesignCon 2012

WHERE CHIPHEADS CONNECT

Donald Telian is an independent Signal Integrity Consultant. Building on over 25 years of SI experience at Intel, Cadence, HP, and others, his recent focus has been on helping customers correctly implement today's Multi-Gigabit serial links. His numerous published works on this and other topics are available at his website siguys.com. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling, and has taught SI techniques to thousands of engineers in more than 15 countries.



- Pre-Hardware Methodology
  - Hitachi Disk
  - IBM SerDes
- 1st 6 Gbps SAS
- 1st AMI Paper
- 2 Paper Awards
- 7-Step Process



UBM Electronics

Industry Bias

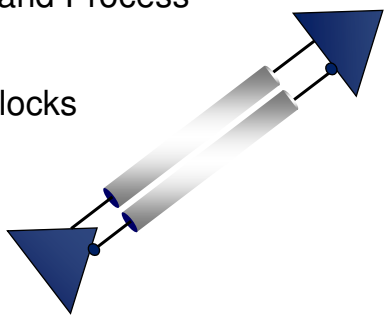
Pre-Hardware

Post-Hardware

- While confirming performance on physical hardware is important
  - And there's lots of investment in this
- There's much to gain figuring out how to do that pre-hardware
  - Challenging since many specs/standards assume post-hardware

Agenda

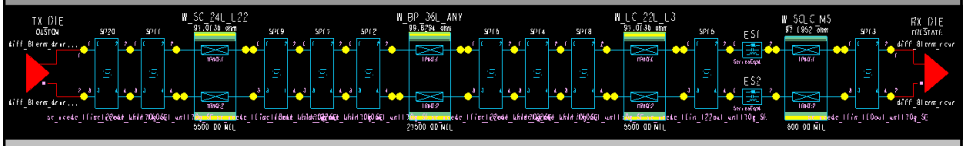
- System-level
  - Adding Active Models
  - Analysis Techniques and Process
- Concepts
  - Necessary Building Blocks



Serial Link Channel Models

Tx Pkg	Backplane Connector	Backplane Connector	Vendor Supplied S-Params	Rx Pkg

Transmission Line Models	Tx Stripline Route	Bp Stripline Route	Rx Stripline Route	Rx Microstrip Route

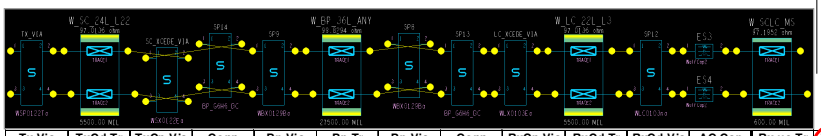


Tx Pkg Via	Tx Conn Via	Bp Conn Via	Bp Conn Via	Rx Conn Via	Rx Cap Via	Field-solved S-Param/Subckts

Tx Model	SPICE / AMI / Experience -based Models	Cap Model	Rx Model

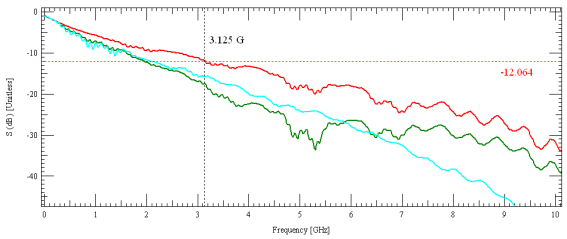
- 17 cascaded elements allow exploration and tuning of channel across 3 PCBs
  - 10 of these are S-parameters
- Valuable work can be done with generic/approximate SerDes models

Passive Channel Loss

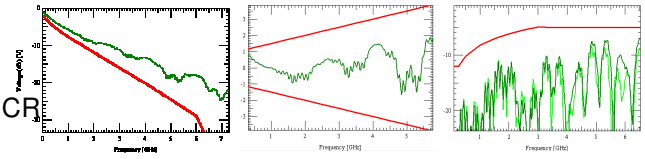


Tx Via	TxCd Tr	TxCn Via	Conn	Bp Via	Bp Tr	Bp Via	Conn	RxCn Via	RxCd Tr	RxCd Via	AC Cap	Rx us Tr	Total dB
0.12	1.97	0.21	0.51	0.40	5.38	0.40	0.51	0.31	1.97	0.12	0.01	0.20	12.11

- Good models =
- Correct loss =
- Right Amplitude =
- Correct Eye



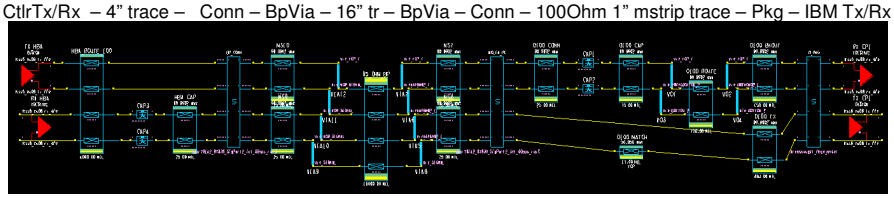
- SSE21 ≠ SDD21

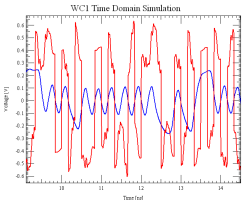


- Industry Masks
  - IL, ILD, RL, FA, ICR

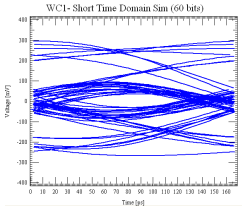
Adding Active Tx/Rx Models

CtlrTx/Rx – 4” trace – Conn – BpVia – 16” tr – BpVia – Conn – 100Ohm 1” mstrip trace – Pkg – IBM Tx/Rx

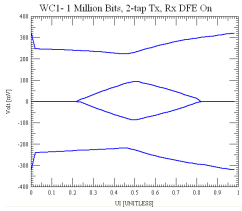




Voltages, System Loss, Time Delay Reasonable



Short TD Eye at Rx Input Mostly Collapsed



Eye Re-opened, AMI Model, Rx DFE Functioning

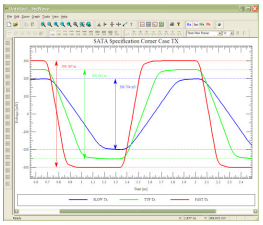
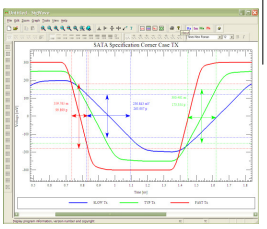
Types of Active Models

- Transistor-Level
- IBIS
- IBIS-AMI
- AMS / Verilog-A
- “Spec” Models

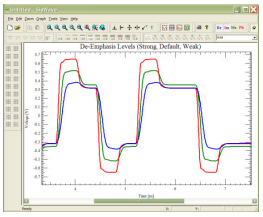
- Native to IC design
- Unwieldy with lots of EQ
- Ok for 2-tap Tx & analog Rx
- Handles EQ complexity
- Fast simulation
- Gaining support / momentum
- Highly configurable, but…
- Valuable, flexible
- Can implement in any format

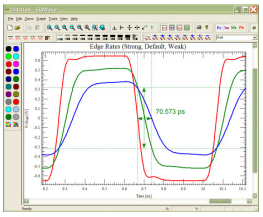
"Spec" Models

SATA Spec
Voltage Swing &
Edge Rates

~PCI Express
Voltage Swing &
Edge Rates

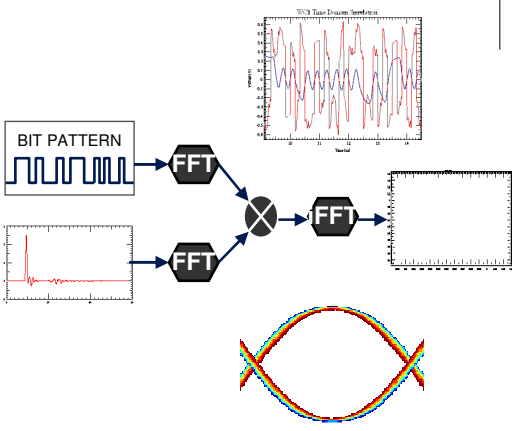




- Craft from base set of parameters in Specs
- Covers range of spec-compatible devices

Types of Serial Link Analysis

1. SPICE .tran
2. Convolution



3. Statistical

4. Peak Distortion Analysis, PDA
   (Worst bit-pattern)

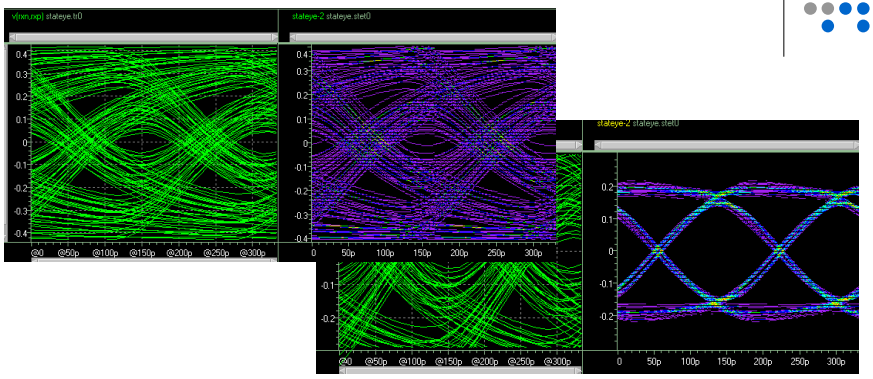
01011111101010100011110010101010000

Technology Comparison

Name	Technology	Pro	Con	Data Pattern	Sim Speed	Max #bits
SPICE	timestep nodal equations	uses silicon model	very slow simulation	any	very slow	~1,000
Convolution	FFT - iFFT	outputs td waveforms	slower than statisical	any	medium	~10,000,000
Statistical	probability functions	calculation of BER	random data pattern	random	fast	no limit
PDA	worst bit pattern	pattern for SPICE	not widely adopted	finds worst	fast	na

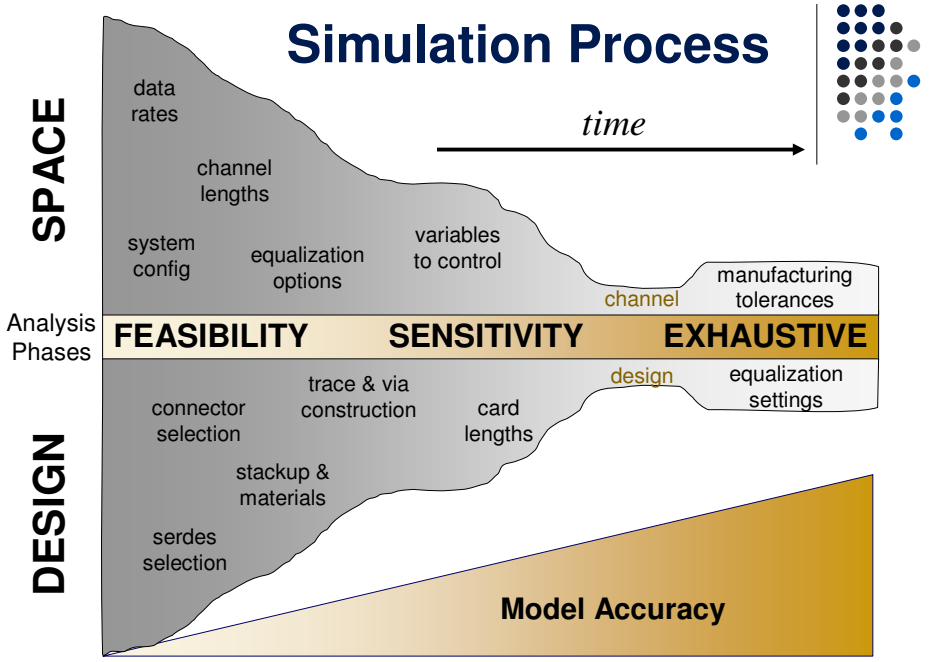
- In the short term, you'll need to understand each solution and work with all of them

SPICE / Conv-Stat Correlation



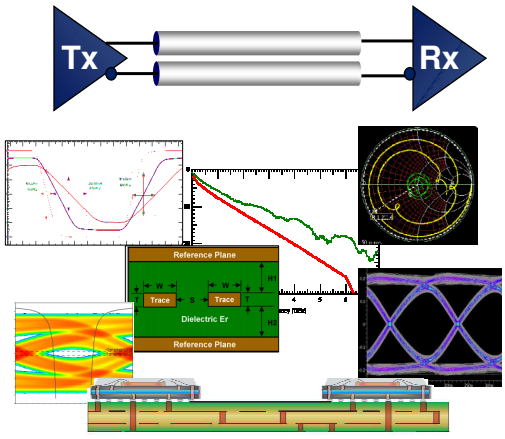
- Initially, hard to move beyond SPICE .tran
  - Helpful to correlate techniques
  - Convolution/Statistical yields smaller eye from more bits
- Once transitioned, LOTS of new capabilities

Simulation Process



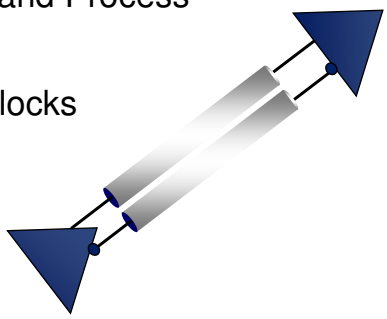
Putting it all Together

- Concepts
- Models
- Simulation
- Design
- Analysis
- Process
- Standards
- Compliance
- Sign-off



Agenda

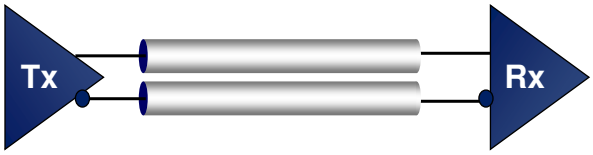
- System-level
  - Adding Active Models
  - Analysis Techniques and Process
- Concepts
  - Necessary Building Blocks



Conceptual Building Blocks

- Differential Signal
- Tx/Rx SerDes
- Serial Link
- Eye
- BER
- Jitter
- Equalization
- Discontinuities

Elements in a Serial Link



Transmitter Channel Receiver

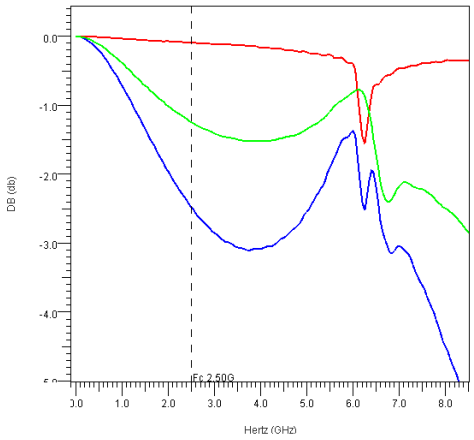
All Serial Links use these 3 items to transmit a differential signal

Why Differential Signaling?

- Really, all signals are “differential”
  - Meaning, they are referenced to something
    - Typically “Ground”
- A “Differential Signal” carries its own reference
  - “Ground” is increasingly an inconsistent reference
    - Across systems, cables, split planes, ground bounce
- Other advantages typically cited
  - Less crosstalk, pwr/gnd rail noise, EMI
  - P/N coupled to each other, less to return path
  - Better for long distances at lower cost

Example: Connector Loss

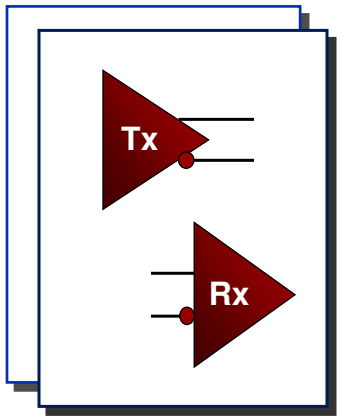
- SDD21
  - Differential
- SSE21
  - Single-ended
- SCC21
  - Common



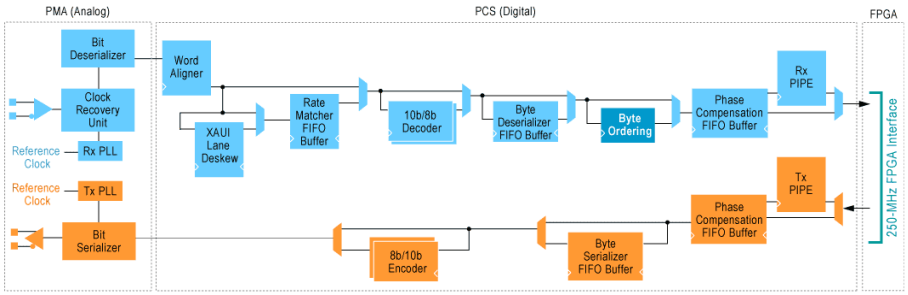
SAS Connector Model Courtesy Amphenol TCS

Understanding Analog Tx/Rx

- The simple IO had a set of characteristics
  - Imped (VI), T_r/f (VT)
- And the differential Tx and Rx do too
  - V_swing, T_rf, V_cm, R_term, Pre-emp%
- Same Tx/Rx handles multiple standards
  - Often programmable



SerDes = Serializer/Deserializer



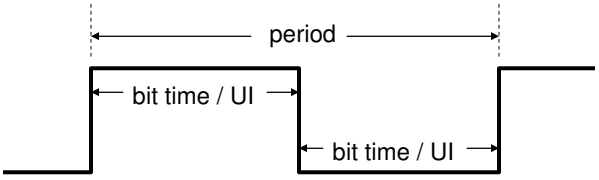
source: http://www.altera.com/products/devices/stratix2gx/features/transceiver/s2gx-mgt-transceiver.html

- Some may use the term for Analog portion only
- Hundreds of times more silicon area than a simple digital I/O

Serial "Link"

- Typically
  - "Channel" = one Tx to Rx connection (half duplex)
  - "Lane" = one channel in each direction (full duplex)
  - "Link" = one or more lanes for serial communication
- "Serial" means single bits flow from Tx to Rx

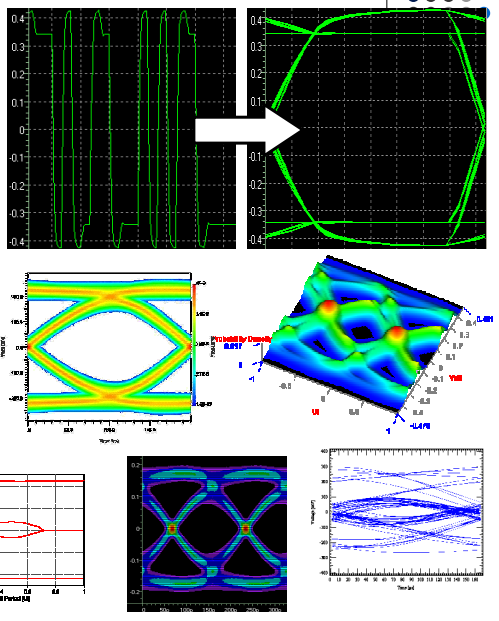
Frequency



- 2 bits = One cycle/period, hence
- Maximum Frequency = ½ Data Rate
  - For example, a 6 Gbps link operates at 3 GHz max
    - There's way too much confusion about this
- This is further confused by "12 Gbps" links that are actually 4 x 3 Gbps lanes in parallel

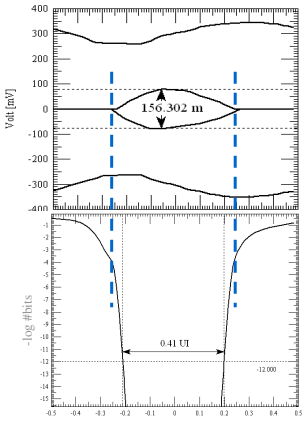
Eye Diagram

- Wraps a time domain waveform back on itself
  - Every "bit time" or Unit Interval (UI)
    - Assuming an ideal (recovered) clock
- Many eye formats
  - Time domain
  - Contour
  - Density (2D, 3D)

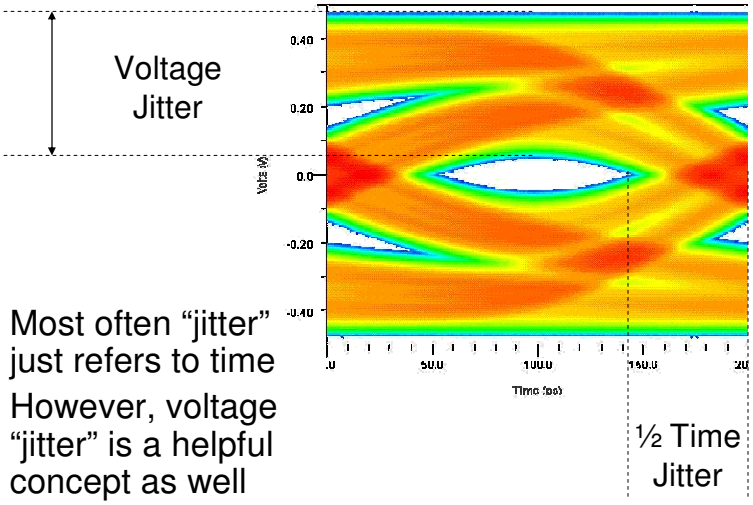


Eye = Baseline Channel Metric

- Standard Metrics
  - Rx Eye Height (mV)
  - Rx Eye Width (UI or pS)
- Capture ~million bits
  - Get beyond knee
- Statistical jitter sources
  - Width at 1e12 bits
- Baseline metric
  - Ht/Wd, mV/UI, 156/0.41
- Often, only Tj is given
  - Wd = UI - Tj

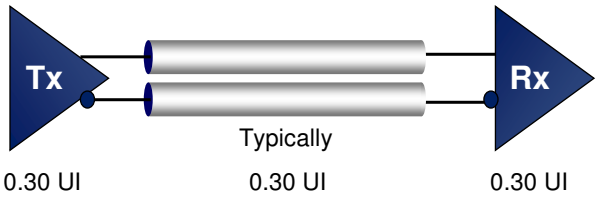


Jitter – Other Side of Ht/Wd



- Most often "jitter" just refers to time
- However, voltage "jitter" is a helpful concept as well

Serial Link Jitter



- Total (Tj)
- Deterministic (Dj)
- Random (Rj)
- Sinusoidal (Sj / Pj)
- Duty Cycle Dist (DCD)
- Various others (?!)

Using Tx Rj in Simulators

- Most tools expect a 1σ/RMS value (Rj_rms)
  - Typically 0.005 UI to 0.015 UI (or, 0.5-1.5 %UI)

> Physical scientists often use the term "root mean square" as a synonym for standard deviation when referring to the square root of the mean squared deviation of a signal from a given baseline or fit. [citation needed] This is useful for electrical engineers in calculating the "AC only" RMS of a signal. Standard deviation being the root mean square of a signal's variation about the mean, rather than about 0, the DC component is removed (i.e. RMS(signal) = Stdev(signal) if the mean signal is 0).
>
> http://en.wikipedia.org/wiki/Root_mean_square#Relationship_to_the_arithmetic_mean_and_the_standard_deviation

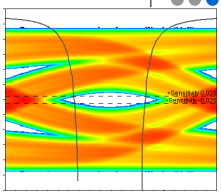
- Many datasheets specify a peak-to-peak value (Rj_pp)
  - Typically 0.07 to 0.21 UI
- At a BER of 10e-12: Rj_pp = 14.069 * Rj_rms
- An incorrect Rj value causes inaccurate simulations
  - Very important to enter this correctly

BER = Bit Error Rate

- Related to Rx eye
- System-level measure of link performance
  - Also CER (Character) and FER (Frame)
- Simply put: #Bit_Errors / #Bits
  - Some times called “Bit Error Ratio”
- Targets are very small values
  - Typically 1e-12
  - Or, 1 error in 1 Terabits
- In time, @ 3 Gbps
  - Longer, for higher confidence

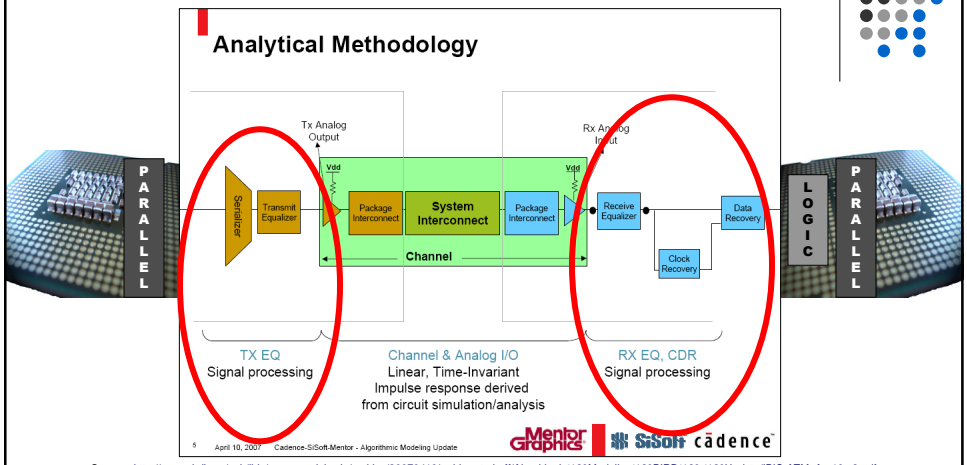
BER	Time
1e-12	5 Minutes
1e-15	4 Days
1e-17	1 Year

Pre-Hardware Simulation



- Most standards stress the Rx
  - And then measure/confirm BER
  - This is a post-hardware methodology
- To do this in simulation, you need:
  1. System-level model of channel (S-params, etc.)
  2. Accurate Tx / Rx models with all EQ stages
  3. Simulation tools that use the full models and show the Rx eye shape against #bits and/or probability
  4. Clear statements from the SerDes Rx vendor regarding eye requirements at the Rx latch and how that relates to a BER
- SerDes vendors typically need to be pushed to provide this data (tie delivery to a PO?)

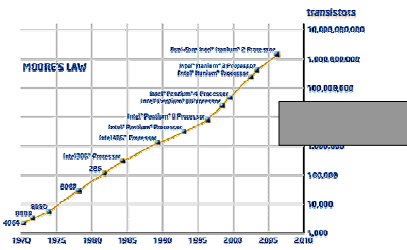
Link Equalization



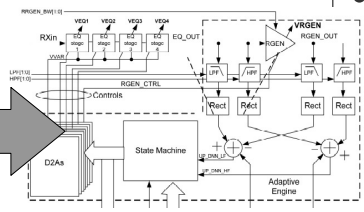
Source: http://www.vhdl.org/pub/ibis/macromodel_wip/archive/20070410/toddwesterhoff/Algorithmic%20Modeling%20BIRD%20-%20Update/IBIS-ATM_Apr10-v3.pdf

- There's a lot of gates between serial and parallel
- Communications theory has met the digital IO

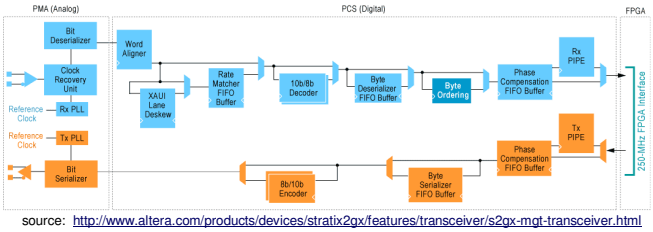
Moore's Law Meets IO Interfacing



source: http://www.intel.com/technology/mooreslaw/index.htm



source: DesignCon 2007 Paper "Digitally Assisted Adaptive Equalizer in 90 nm With Wide Range Support From 2.5 Gbps to 6.5 Gbps" see http://www.altera.com/literature/cp/cp-01026.pdf

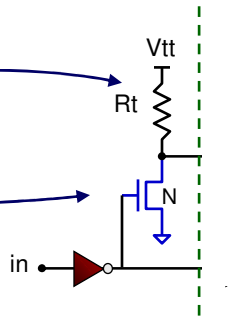


source: http://www.altera.com/products/devices/stratix2gx/features/transceiver/s2gx-mgt-transceiver.html

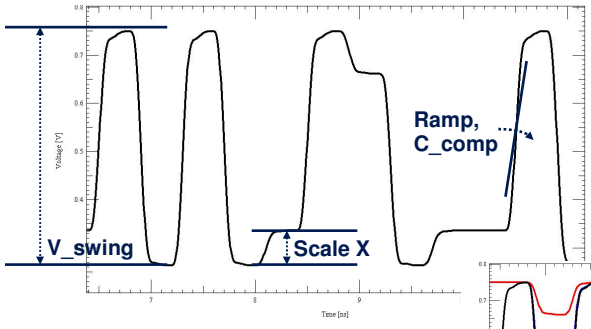
An increasing amount of transistors are consumed by signal transmission
"IC gates are cheaper than PCB traces"

Typical Tx EQ

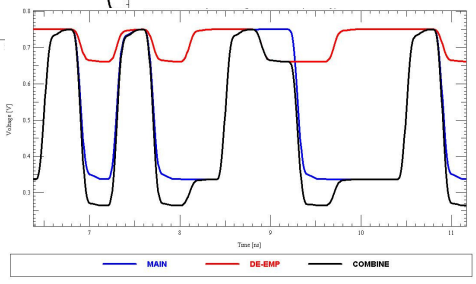
- Normal Tx data
  - Vtt
  - Rt
  - Pulldown VI Curve
  - Ramp rate
  - C_comp
- Additional "taps"
  - Unit interval
  - Pre-emphasis dB, or
    - Scale factor (x)
- Tx Advantage: Signal is known



Parameters in Waveform



- Scaled signal in red is Tx bit pattern inverted and one UI later



- Tx's pre-knowledge of UI and pattern enables better EQ and pre-cursor tap
  - Often makes Tx source better than a re-driver

Parameters in Specs*

PCI EXPRESS™

4.3.3. Differential Transmitter (TX) Output Specifications

The following table defines the specification of parameters for the differential output at all Transmitters (TXs). The parameters are specified at the component pins.

Table 4-5: Differential Transmitter (TX) Output Specifications

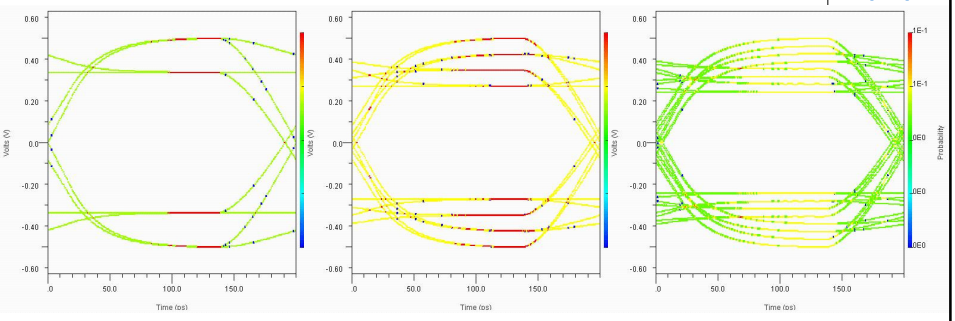
Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps +/-300 ppm. UI does not account for SSC dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.800		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 2.
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125			UI	See Notes 2 and 5.
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential Mode Low impedance
Z_{TX-DC}	Transmitter DC Impedance	40			Ω	Required TX D+ as well as D- DC impedance during all states

*Specs courtesy of PCI Express™ Base Specification 1.0a pages 211 & 212

Tx Parameter:

- **Bit Time**
- **V_swing**
- **Scale Factor**
- **Ramp dt, C_comp**
- **Rt**
- **Rt**

#Taps & Tx FFE Voltage Levels



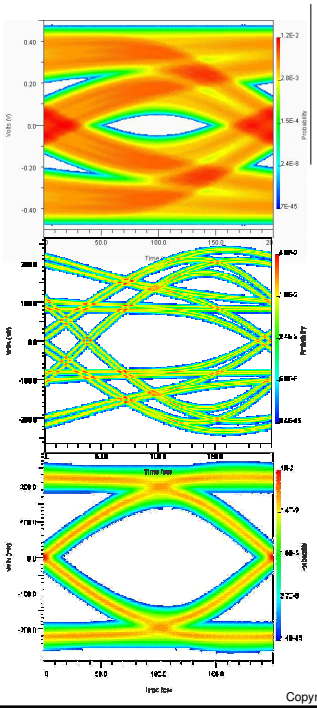
cursor+1 cursor+2 cursor+3

- # levels = 2^X, where x= # of non-cursor taps
- terminology can be confusing (1-tap or 2-tap?)

Tx EQ Balancing

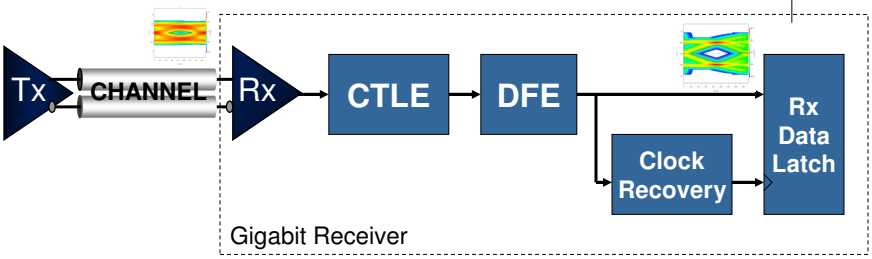
- 2' chan, 1-post Tx, Rx eye
- Under-equalized
  - 115mV/95pS, 414mV/105pS
  - Ht / Wd , V_jit / T_jit
- Over-equalized
  - 144mV/140pS, 170mV/60pS
- Well-equalized
  - 283mV/171pS, 123mV/29pS

Minimizing voltage jitter also minimizes time jitter and helps stabilize system

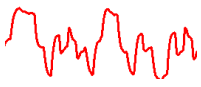


NOTE: Presence of an Rx DFE changes all this

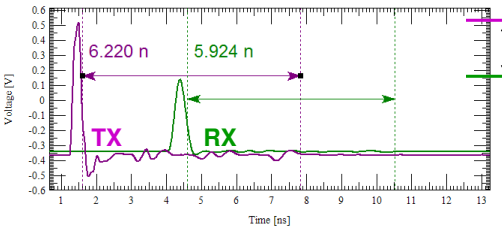
Typical Rx EQ



- Rx EQ is more challenging, data NOT known
- Rx EQ often compensates for >15 dB of loss
  - CTLE = Continuous Time Linear Equalizer
    - Or simply "Linear Equalizer" or "Peaking Filter"
  - DFE = Decision Feedback Equalizer
- Increasingly, signal is measured at "Rx Latch"
  - Since the eye is closed at Rx input



The Impulse Response



Rx ~60% of Tx, or ~ -5dB loss

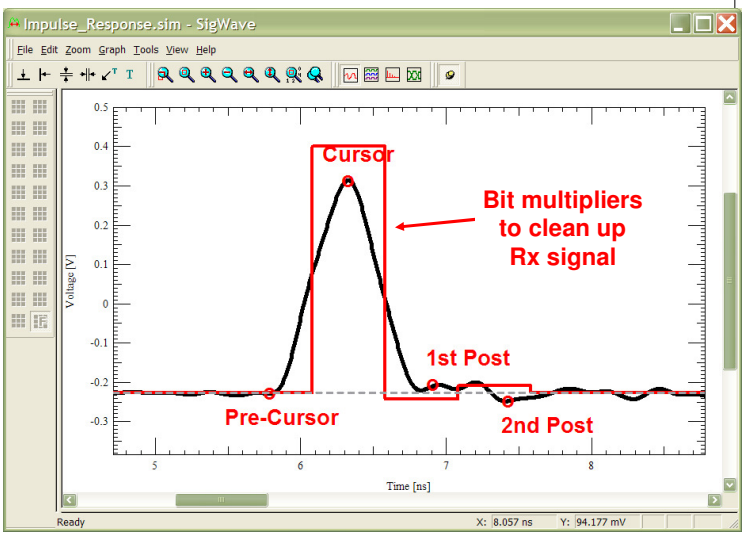
ISP ~6 nS => #bits to sim =

2^(6*2.5) = 2^15 = 30k (2.5Gbps)

2^(6*3.125) ~= 500k (3.125 Gbps)

- System interconnect's "fingerprint"
- Reveals Tx to Rx "loss" (similar to eye or S_21)
- Reveals "Interconnect Storage Potential (ISP)"
  - From which we can determine # bits to simulate
  - ISP detailed in Intel/Cadence DesignCon 2005 paper
    http://www.siguys.com/resources/2005_DesignCon_New_MGH_Techniques_ISP_CA_PCIe_SATA.pdf

Impulse Response & "Cursors"



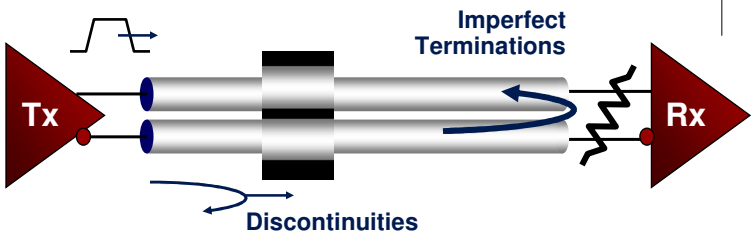
- All non-cursor signal causes ISI

Balancing System EQ

- Only Tx can handle pre-cursor ISI
  - Due to foreknowledge of the bit pattern
- Both Tx FFE and Rx DFE handle post-cursor ISI
  - If Rx DFE is available, don't over-do Tx post-cursor EQ
  - Likely more efficient to intentionally under-equalize
- A clean eye delivered to an Rx pin that has DFE
  - Under-utilizes the Rx DFE
  - Provides the Rx with less signal amplitude to work with
  - Likely wastes power
- System-level view is needed
  - Concept is not intuitive, as signal at Rx pin is not optimized
  - However, eye at Rx Latch is likely improved 100%
  - "Simulating Large Systems with Thousands of Serial Links"

DesignCon 2012Session 8-WA3

Channel Discontinuities

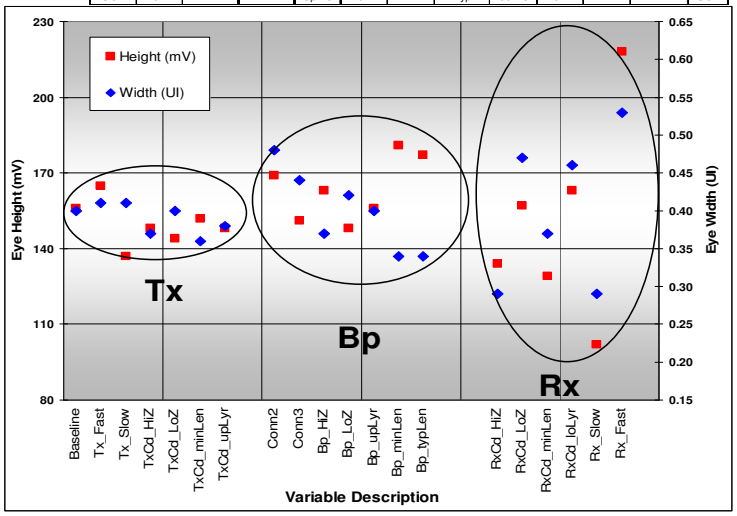


- Tx transmits a bit many bit times before Rx receives the same bit
  - A 20" 6 Gbps channel contains about 20 bits
    - almost as though the channel has "memory"
- Discontinuities cause some amount of energy to bounce around
  - IC packages, PCB traces, vias, connectors, AC capacitors, cables…
- The remaining energy from previous bits interferes with new ones
  - Often called "Inter-symbol Interference" or "ISI" – causes eye closure
- Your task: remove or minimize discontinuities to open eye

PCB Variables: System Relevance

Baseline

Tx Card				Backplane					Rx Card			
Tx	Card	Length	Layer	TxConn	Bp	Layer	Length	RxConn	Card	Length	Layer	Rx
Typ	NomZ	Max	Lower	Conn1	NomZ	Lower	Max	Conn1	NomZ	Max	Upper	Typ
Fast	HighZ	Min	Upper	Conn2	HighZ	Upper	Min	Conn2	HighZ	Min	Lower	Fast
Slow	LowZ			Cpnn3	LowZ		Typ	Conn3	LowZ			Slow



Manage:

Tx

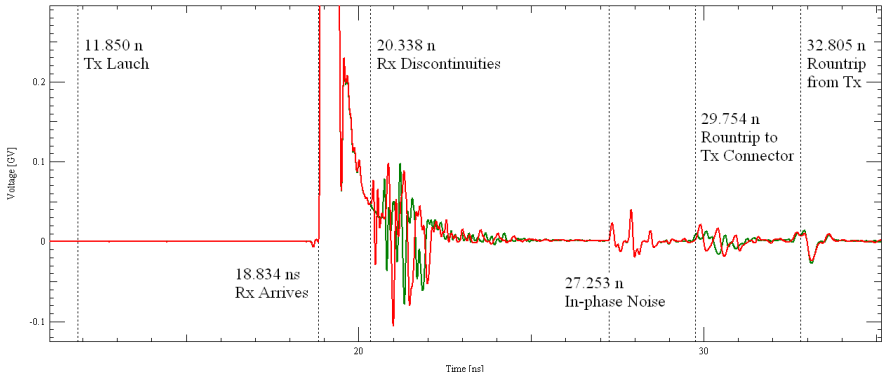
Bp

Rx!

Full paper: http://www.siguys.com/resources/2010_DesignCon_6GbpsSimTechniques_Paper.pdf

Manage Rx Discontinuities

- Impulse response of two same-length channels
- Red (short Rx len) eye 20% worse than green (long Rx len)



- Minimize via stubs, design AC cap structure
- Enforce minimum length: 40% more margin!

Summary

- S-Parameters model passive structures
- System simulation adds active models
- Eye opening is primary metric
- Use of equalization growing
- Post-hardware bias fading
- New process emerging

DesignCon 2012

WHERE CHIPMAKERS CONNECT

For More Info

"Simulating Large Systems with Thousands of Serial Links"

While not long ago a serial link was only a couple of wires, it's now becoming common for systems to include hundreds – and even thousands – of such links. This paper describes the development and analysis of a large system with thousands of serial links. Due to the system's size and complexity, the design team invested in a multi-year effort to build and qualify a virtual environment capable of both verifying connectivity and simulating any and all of the channels. Problematic channels with incomplete system-level connections, poor eye openings, or high BER are quickly identified. Performance limiters such as inherent discontinuities, cavity resonances, and Tx/Rx equalization imbalance are found and examined in detail. The virtual system is also used to guide design choices such as layer stacking, via construction, back-drilling, and trace/connector impedances. Processes to optimize and select equalization choices are also described.

SiGuys, Ericsson, SiSoft

8-WA3, Wednesday February 1, 10:15am, Ballroom K

UBM Electronics


DESIGNCON 2012
WHERE CHIPHEADS CONNECT
Questions
SI GUYS
www.siguys.com
UBM
Electronics