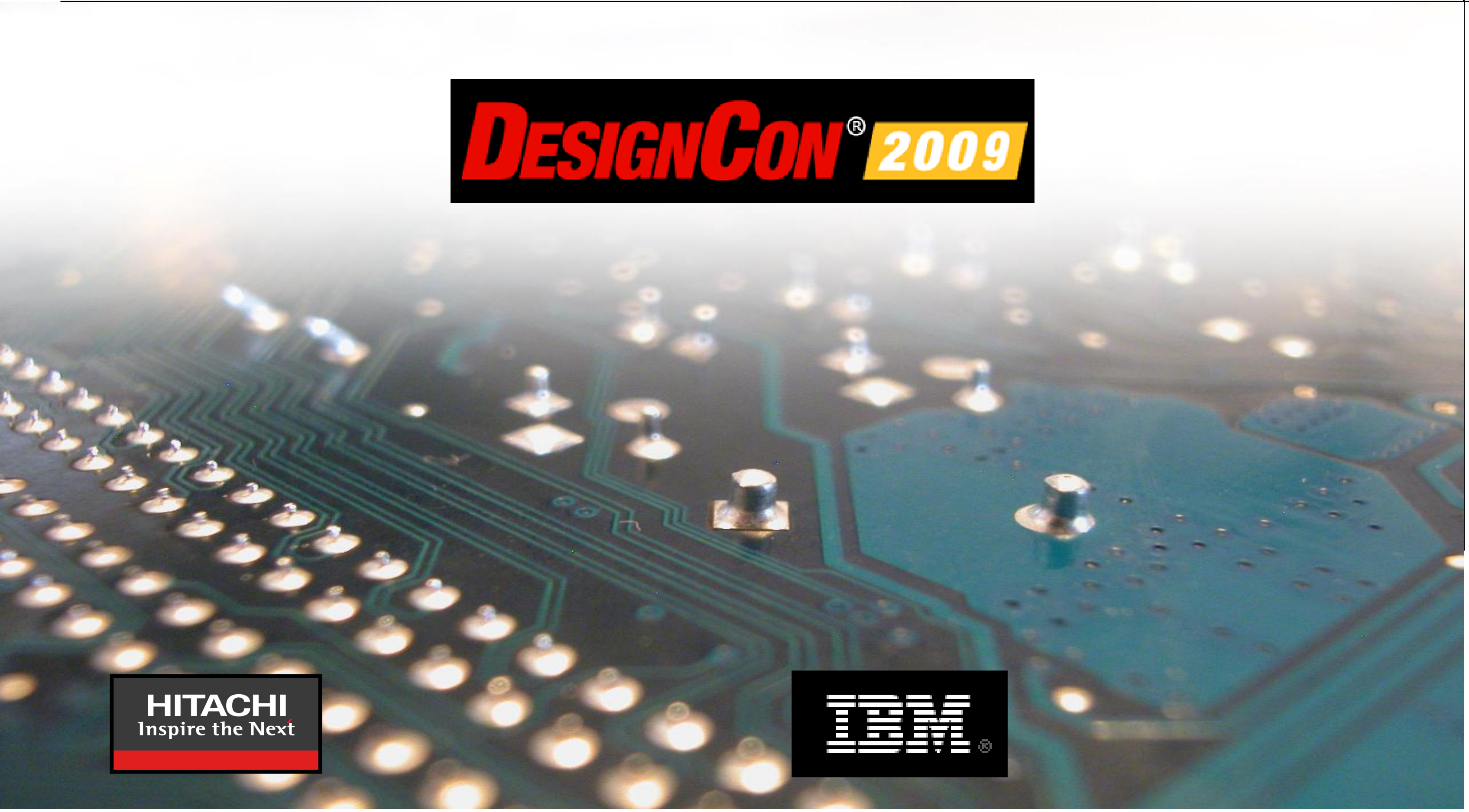
New Serial Link Simulation Process, 6 Gbps SAS Case Study

Donald Telian – SI Consultant

Session 7-TH2



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Donald Telian
SI Consultant

About the Authors

Donald Telian is an independent Signal Integrity Consultant. Building on 25 years of SI experience at Intel, Cadence, HP, and others, his recent focus has been on helping customers correctly implement today's Multi-GHz serial links. He has published numerous works on this and other topics. Donald is widely known as the SI designer of the PCI bus and the originator of IBIS modeling and has taught SI techniques to thousands of engineers in more than 15 countries. Donald can be reached at: telian@sti.net

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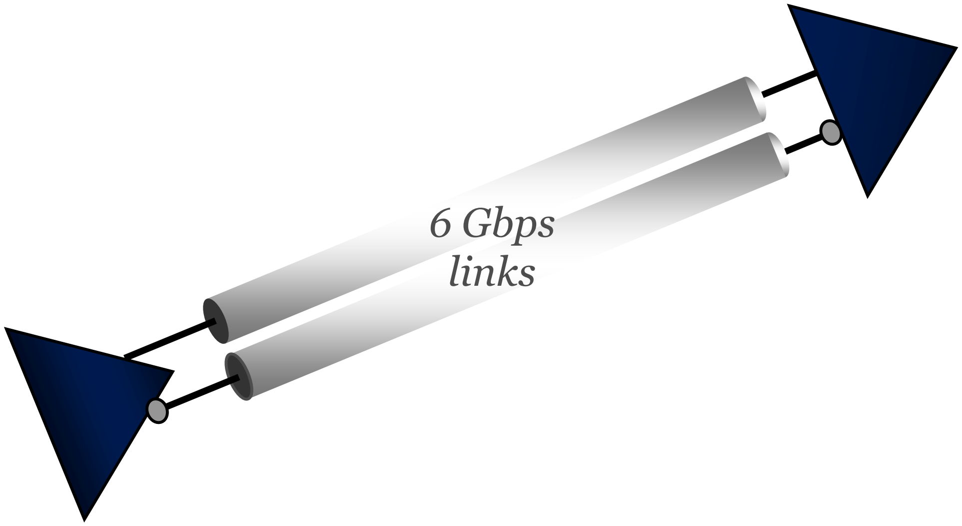
Adge Hawes is a Development Architect for IBM at its Hursley Labs, United Kingdom. He has worked for IBM for more than 30 years across such hardware as Graphic Displays, Printing Subsystems, PC development, Data Compression, and High-Speed Serial Links. He has represented the company in many standards bodies such as PCI, SSA and Fibre Channel. Recently he has moved from Digital Logic to Analog and Mixed-Signal, where he develops simulators for IBM's High Speed Serial Link customers. Adge can be reached at: adge@uk.ibm.com

Agenda

- Intro to Project, Tools, & Technologies
- Verifying SAS Spec Compliance
- Virtual Systems Analysis
- Conclusions



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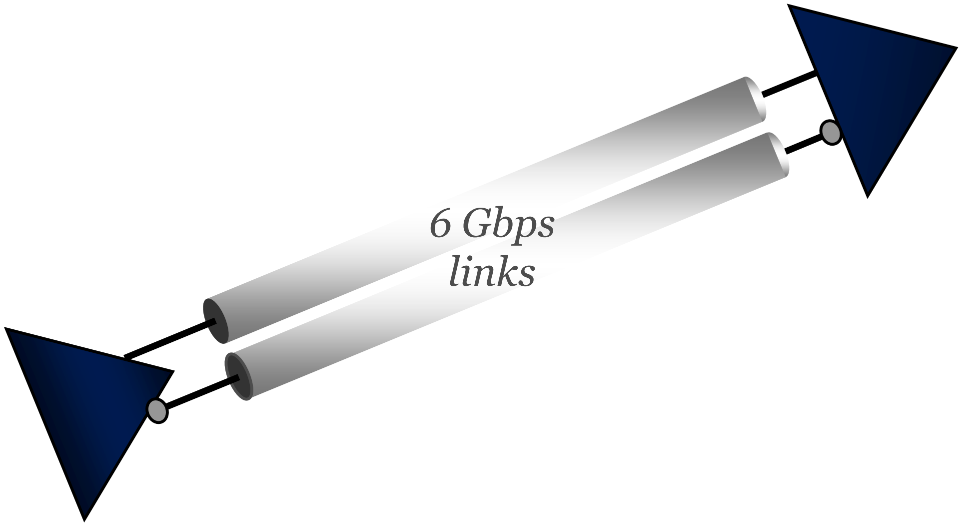
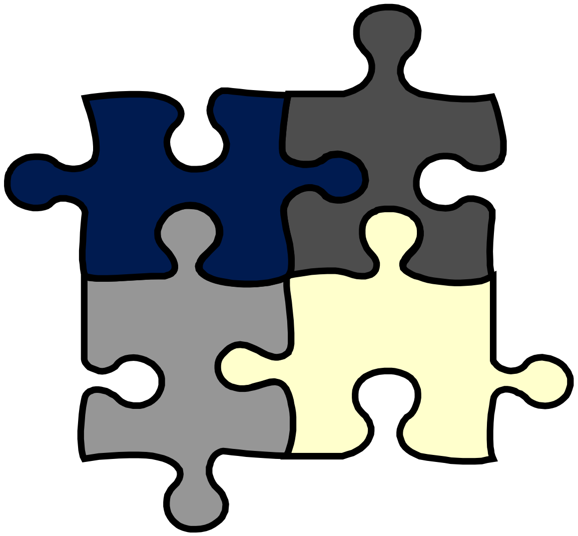


About the Project

- Identify and implement new simulation environment for future 6+ Gbps Hard Disk Drive (HDD) designs
- Prove-in environment on design of future products
- 6 Gbps Challenges
  - Loss ~20dB (10% of Tx signal at Rx)
  - Rx signal un-measurable
  - Complex equalization schemes
  - New model formats (AMI)
  - New simulation techniques
  - New modeling standards emerging
  - Spec compliance requires simulation
- Coordinate ~15 key industry players
  - Customers, suppliers, tool vendors, standards committees

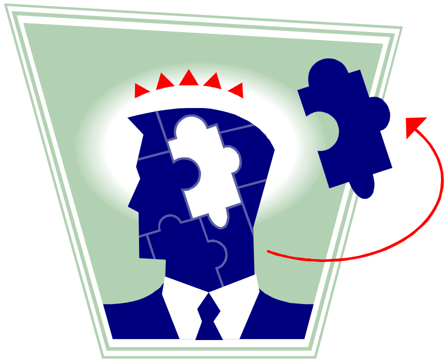


Project Phases

- Assessment
- Proof-of-Concept
- Model Development
- System Analysis
- Kit Environment

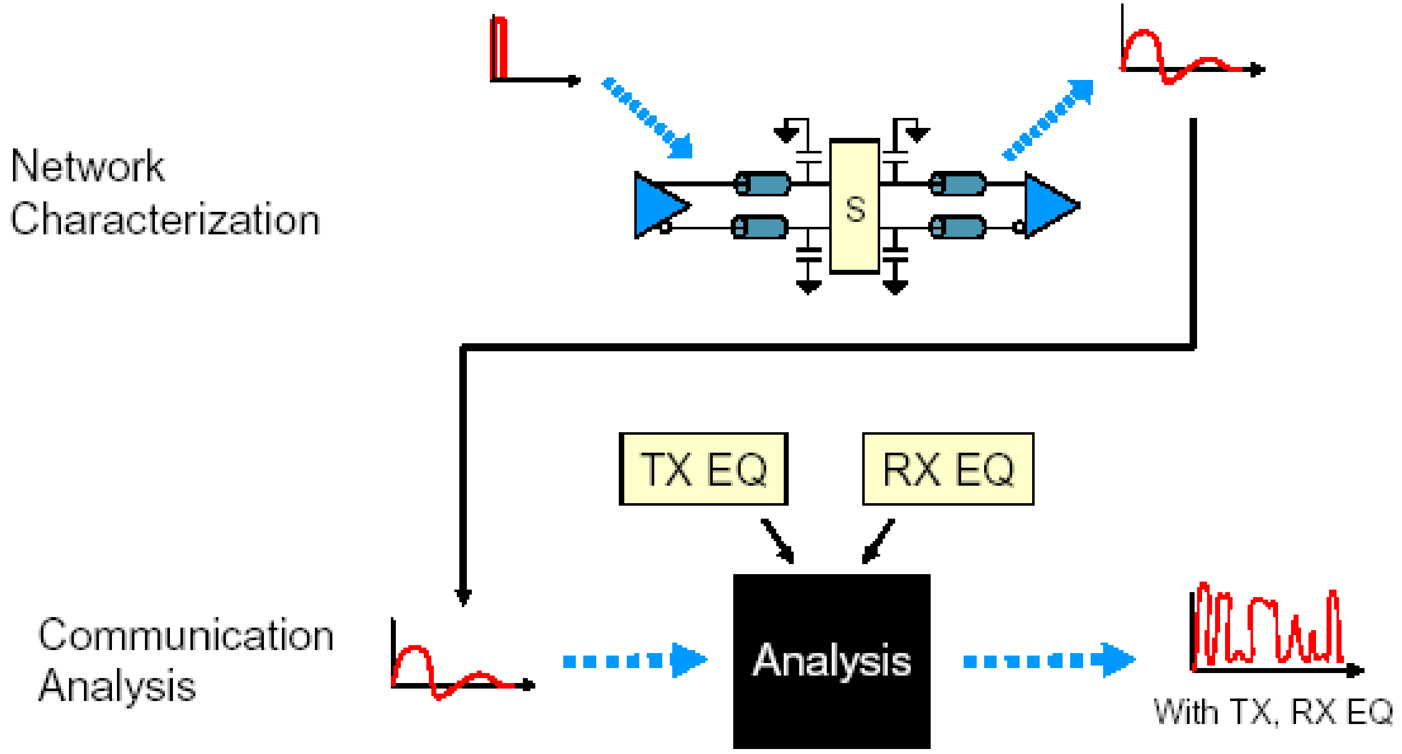
- ~ 6-month Effort

Terminology



- SAS = Serial Attached SCSI
- Serial Link = Channel
- Channel Analysis = Serial Link Simulation
- CA = Channel Analysis = simulation tool
- DFE = Decision Feedback Equalization = Rx Eq
- FFE = Feed-Forward Equalization = Tx Eq
- SerDes = IBM 6 Gbps core, in this case
- AMI = Algorithmic Modeling Interface

AMI Model Review



Circuit Analysis with Existing Models

Algorithmic Models

Image courtesy IBIS-ATM Group and Todd Westerhoff: http://www.vhdl.org/pub/ibis/summits/sep07/

- Algorithmic models typically implemented in .dll files
- AMI format approved by IBIS Committee in Nov. ’07
- More background see: CDNLive! 2007 Session 8.3

Hard Disk Drive Model

SYSTEM

CONN

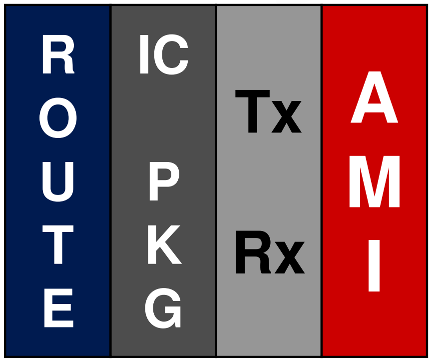
ROUTE

IC PKG

Tx Rx

AMI

=



ROUTE

IC PKG

Tx Rx

AMI

=

HDD

HDD model used with both compliance and system loads

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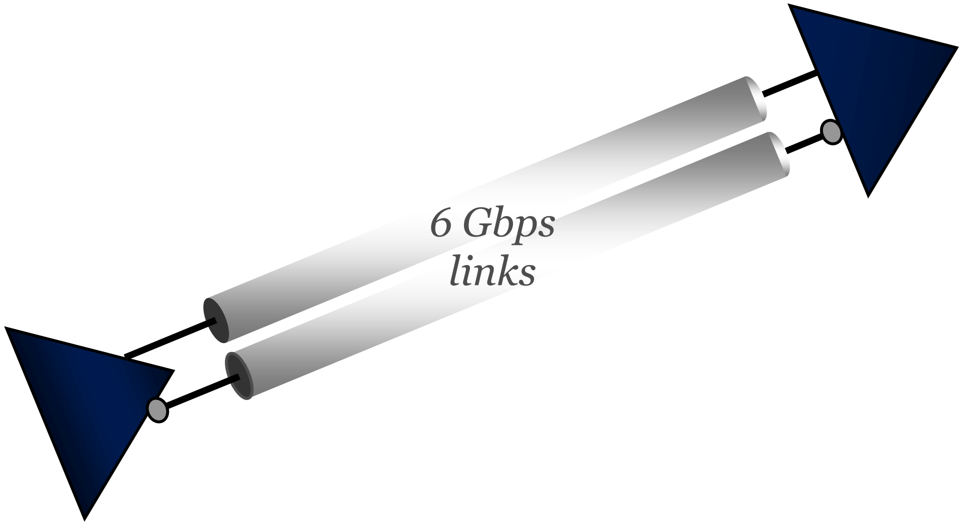
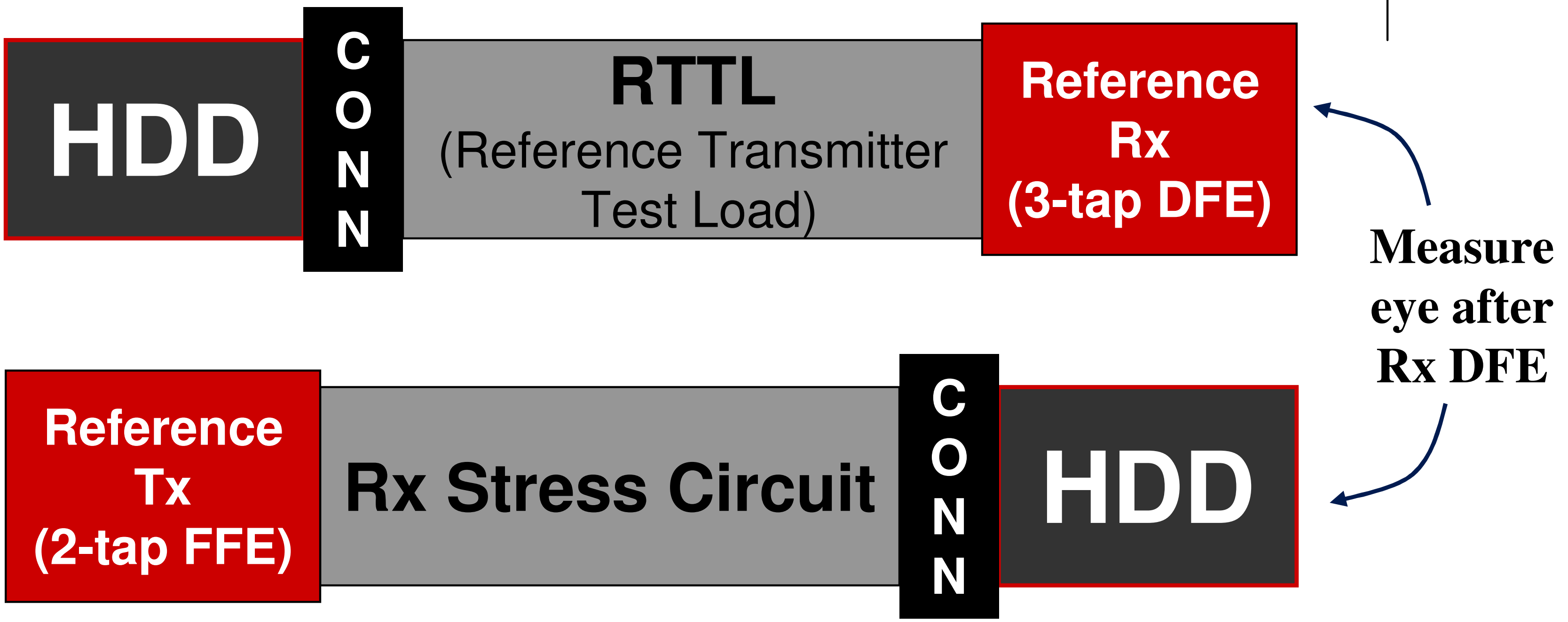


SAS Compliance Testing

- Tx

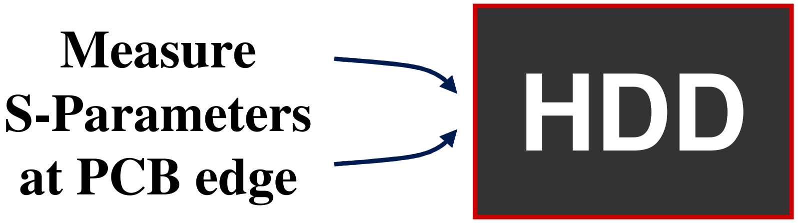
- Rx


HDD
CONN
RTTL
(Reference Transmitter Test Load)
Reference Rx (3-tap DFE)

Reference Tx (2-tap FFE)
Rx Stress Circuit
CONN
HDD

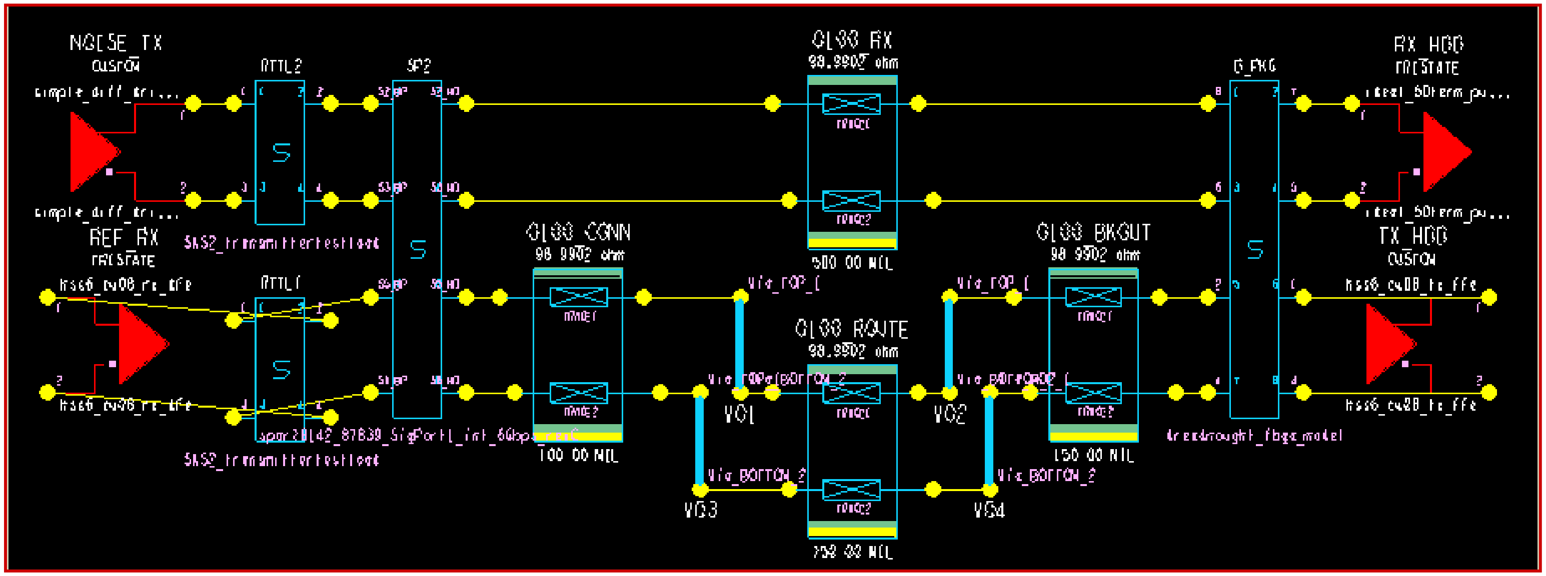
Measure eye after Rx DFE

- Port


Measure S-Parameters at PCB edge
HDD

Tx Compliance Testing

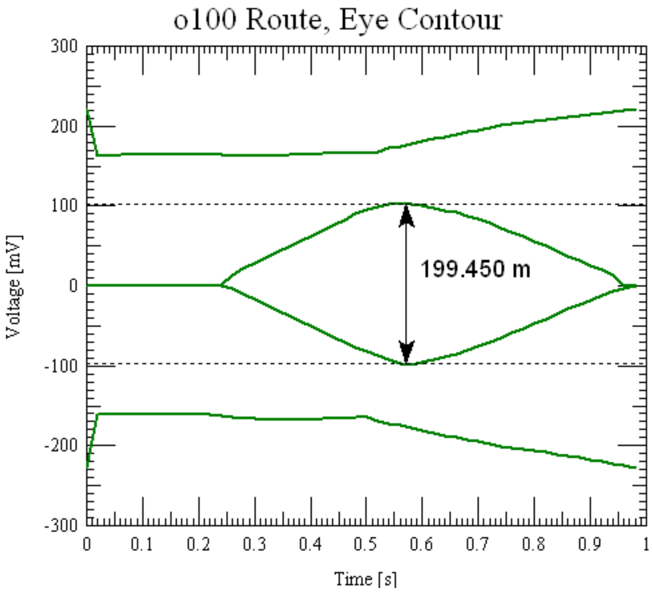
- Simulation specified as only way to validate
  - Eye measured inside IC at output of Rx DFE
  - Spec calls out Reference Rx 3-tap LMS DFE
- Transmit through -15dB “RTTL” S-parameters

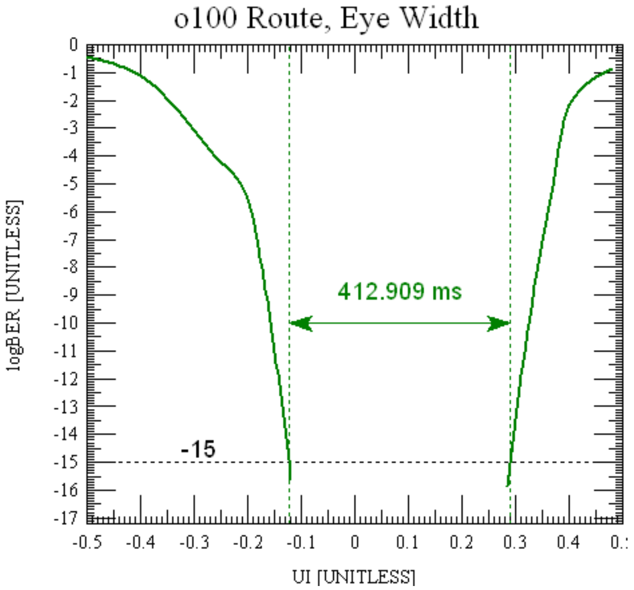


Noise Channel

Channel Under Test

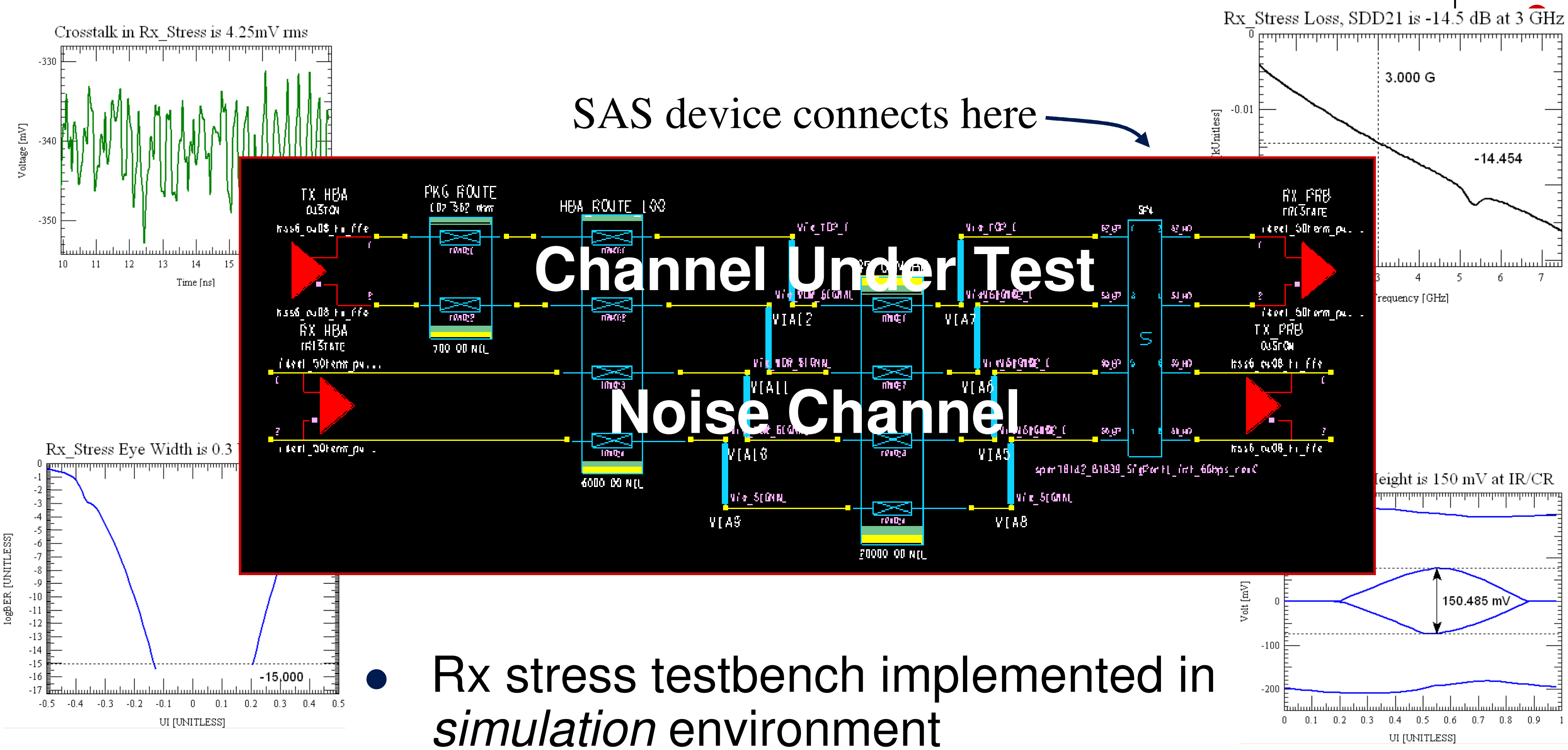
Tx RTTL Simulation Results





- 4 taps configured in Tx, noise channel active
  - Tx set at spec reference levels (nominal EQ)
- Height/width = 179mV/0.41UI (100/0.40 spec)
- Comfortable with small margin on width

Rx Compliance Testing



SAS device connects here

Channel Under Test

Noise Channel

Crosstalk in Rx_Stress is 4.25mV rms

Rx_Stress Loss, SDD21 is -14.5 dB at 3 GHz

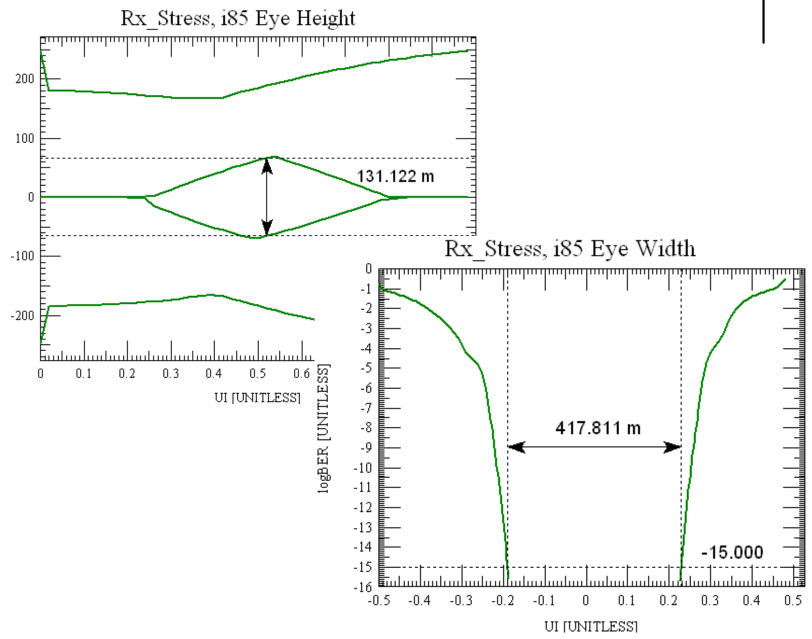
Rx_Stress Eye Width is 0.3

Eye Height is 150 mV at IR/CR

- Rx stress testbench implemented in *simulation* environment
- Delivered crosstalk, loss, eye w/h, from Reference Tx as specified

Rx Stress Test Results

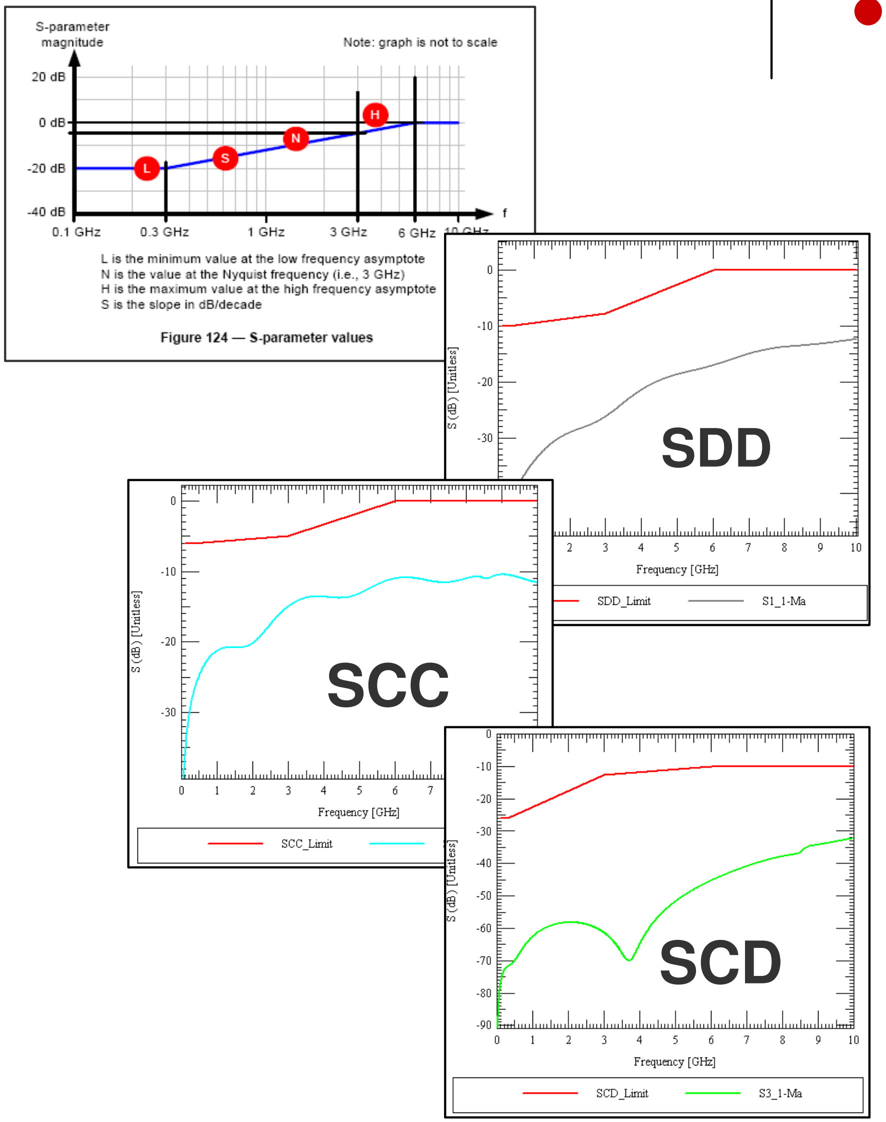
- Two HDD route styles tested
  - 100 Ohm microstrip
  - 85 Ohm stripline
- Eye height & width measured at 1e15 bits
  - height extrapolated
- Derive design margins
- Guide design choices



Parameter	**o100**	**i85**	**Unit**
Eye Height (1e6 bits)	108	131	mV
Eye Height Margin (60mV - 10%)	**37**	**58**	mV
Eye Width (1e15 bits)	0.408	0.418	UI
Margin in UI (target = 0.2 UI min)	0.208	0.218	UI
Margin in pS	**35**	**36**	pS

S-Parameter Limit Compliance

- Differential nets extracted for virtual VNA measurement
- Plot SDD, SCC, SCD against specified limits (in red)
- All measurements below limits



L is the minimum value at the low frequency asymptote
N is the value at the Nyquist frequency (i.e., 3 GHz)
H is the maximum value at the high frequency asymptote
S is the slope in dB/decade

Figure 124 — S-parameter values

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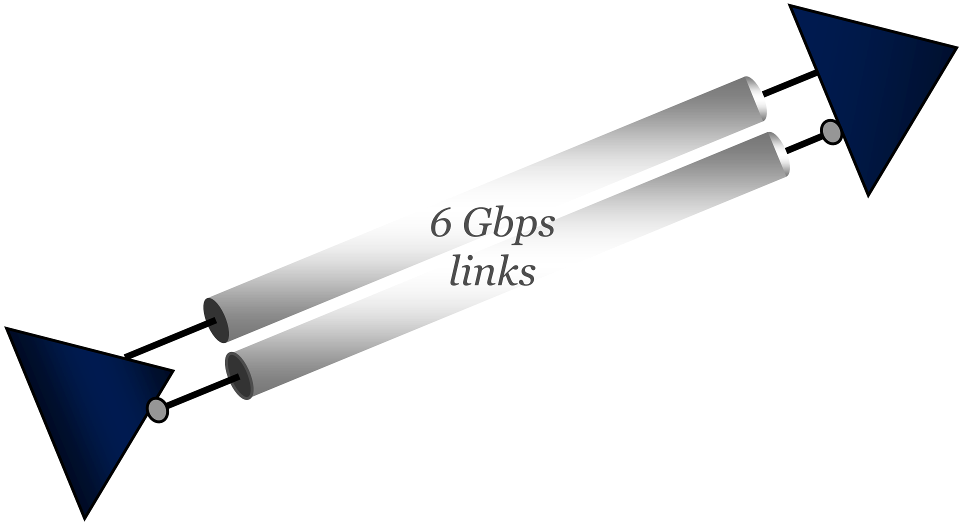
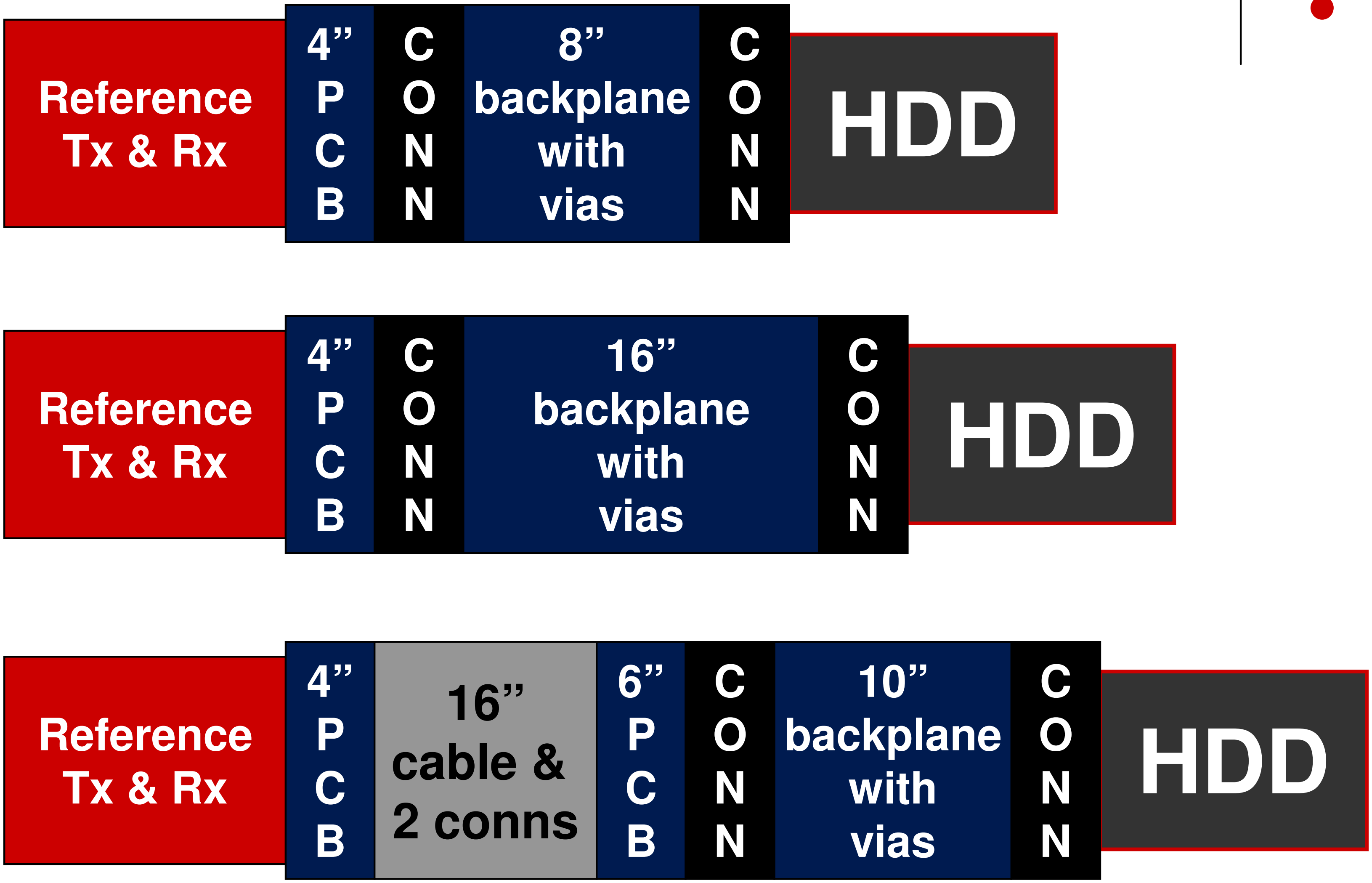


System Configuration Testing



- TYP

Reference Tx & Rx

4" PCB

CONN

8" backplane with vias

CONN

HDD

- WC1

Reference Tx & Rx

4" PCB

CONN

16" backplane with vias

CONN

HDD

- WC2

Reference Tx & Rx

4" PCB

16" cable & 2 conns

6" PCB

CONN

10" backplane with vias

CONN

HDD

System Configuration Metrics

Parameter	**TYP**	**WC1**	**WC2**	**Unit**
PCB & Cable Length	13	21	37	inches
# of Connectors	2	2	4	#
# of Vias	4	4	4	vias
Propagation Time	2.5	4	6	nS
6 Gbps bits in channel	15	24	36	bits
Channel Loss (SDD21 @ 3 GHz)	-8.9	-13.6	-16	dB

- Apply experience to augment spec’s coverage
- Acquire intuitive sense of what works, what doesn’t
- Wide range of length, loss, discontinuities
- Drive with minimal Tx, recover signal with IBM DFE

7-Step Link Analysis Process

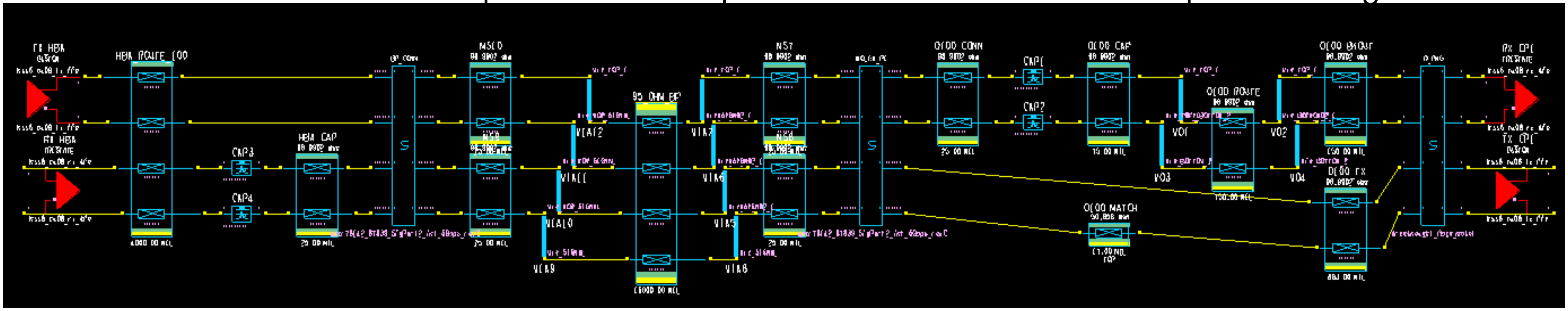
Step	Task	Purpose	Output
1	Collect & Connect Models	Build Link Model	Link Ready-to-Run
2	Model Sanity Check	Verify Model	TD Functional
3	Quantify Loss & Crosstalk	Understand & Gauge Link	S21 dB, mV RMS
4	Plot Impulse Response & ISP	Measure ISP, Calculate #bits	#bits for CA
5	Verify Eye Convergence	Test #bits, Confirm Coverage	CA Functional
6	Parameter Determination	Setup for Worst-Case	CA Parameters
7	Corner Case Analysis	Derive Design Margins	Eye h/w Margins

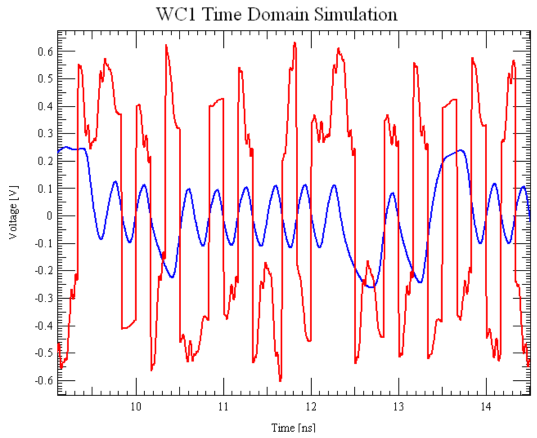
Illustrate on WC1 channel (TYP & WC2 in paper)

Can be applied to any serial link SI analysis

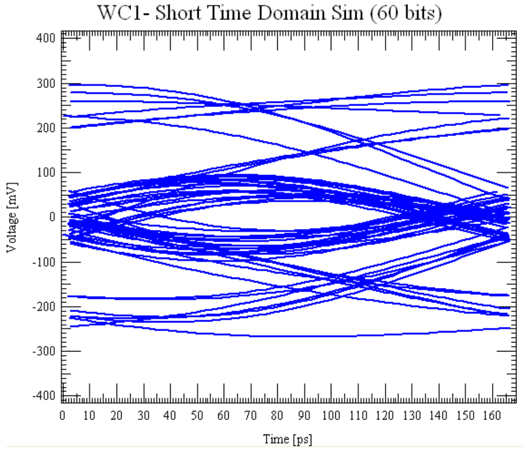
Step 1: Collect & Connect Models
Step 2: Model Sanity Check

CtlrTx/Rx – 4” trace – Conn – BpVia – 16” tr – BpVia – Conn – 100Ohm 1” mstrip trace – Pkg – IBM Tx/Rx

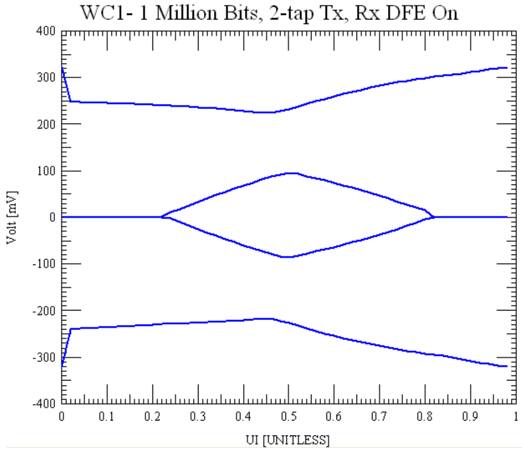




Voltages, System Loss, Time Delay Reasonable

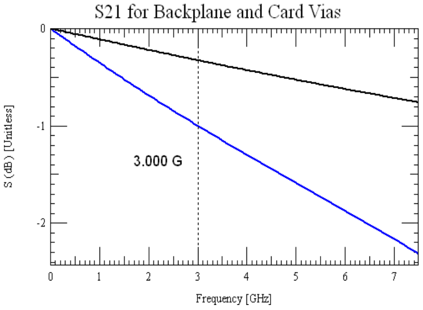


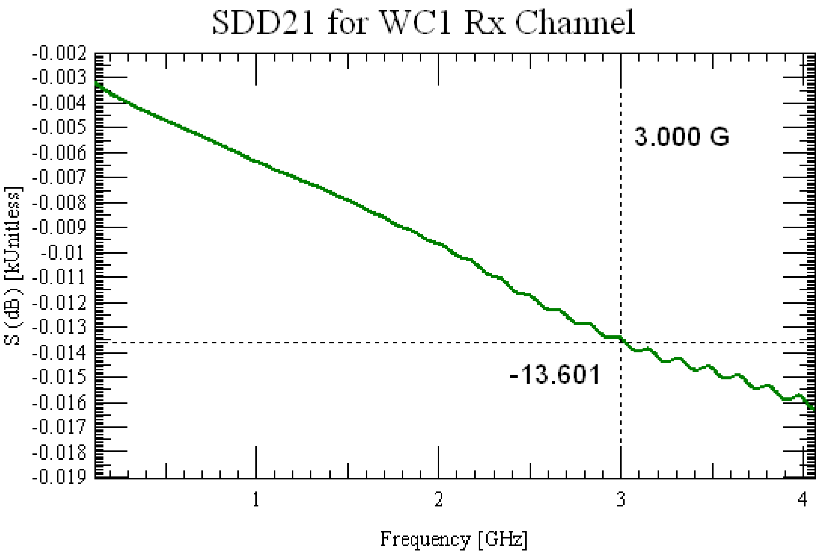
Short TD Eye at Rx Input Mostly Collapsed

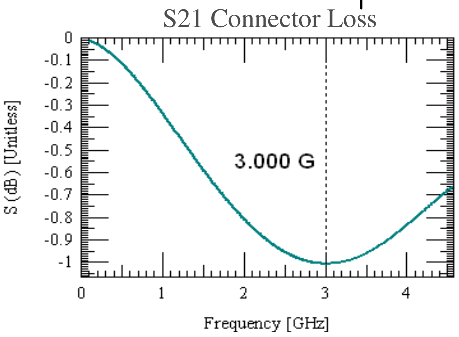


Typical CA Eye Re-opened, Rx DFE Functioning

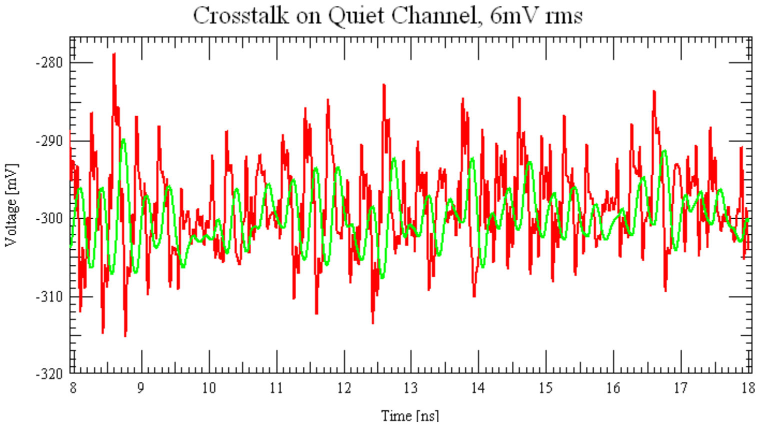
Step 3: Quantify Loss & Crosstalk


S21 for Backplane and Card Vias


SDD21 for WC1 Rx Channel


S21 Connector Loss

Total Loss = 2*BpVia + 2*CdVia + 2*Conn + 21”*0.33dB/inch + Misc
Hand Calculation = 2*1 + 2*0.3 + 2*1 + 21/3 + 2 = 13.6dB


Crosstalk on Quiet Channel, 6mV rms

Crosstalk = 5.6 mV rms

Step 4: Plot Impulse Response & ISP
Step 5: Verify Eye Convergence

- Impulse Response shows noise to ~8nS
- Interconnect Storage Potential (ISP) = 1.6 nS
- Bit affected by 10 bits previous (1 symbol)
- Eye converges ~1e5 bits
- #bits parameter for CA
- ISP defined in [this paper](http://www.t11.org/ftp/t11/pub/fc/fcsm2/05-215v0.pdf)

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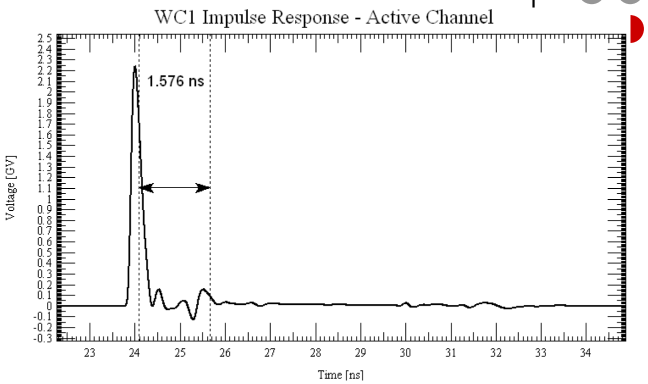

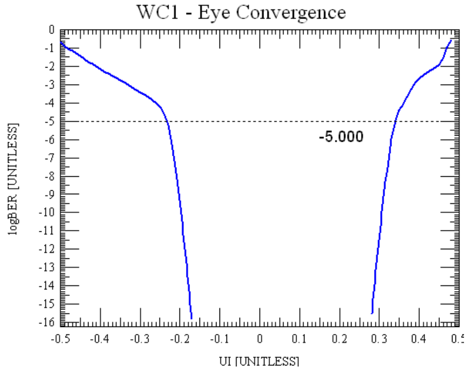

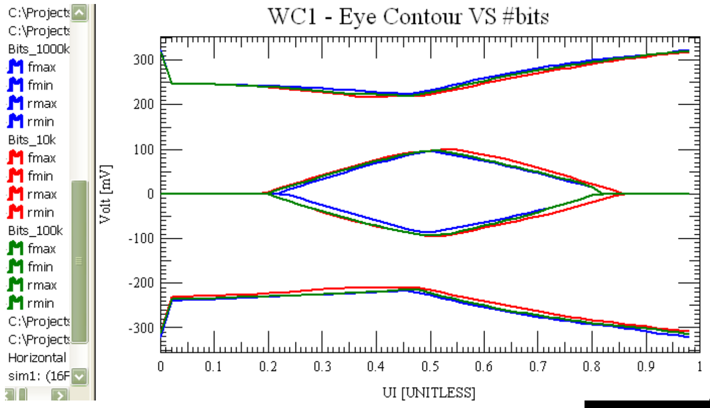

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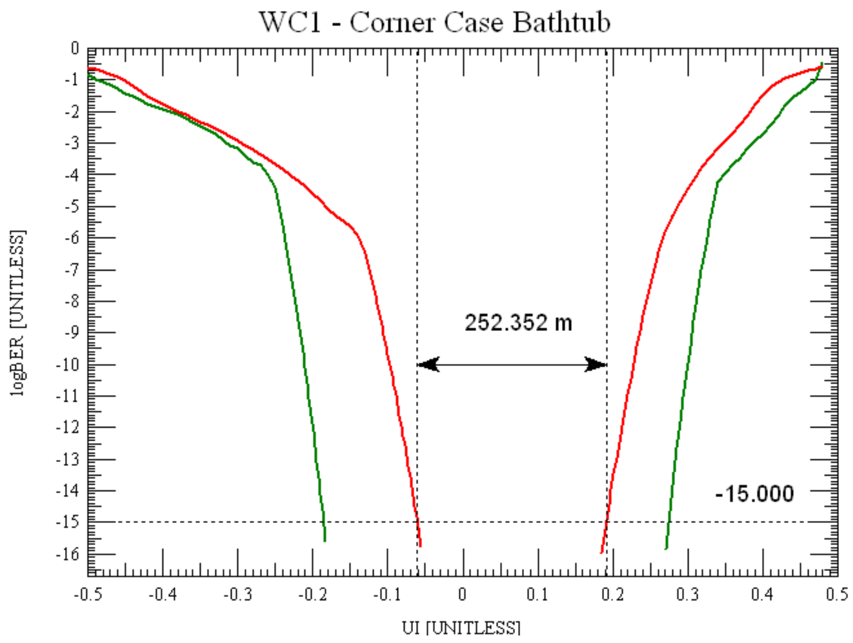
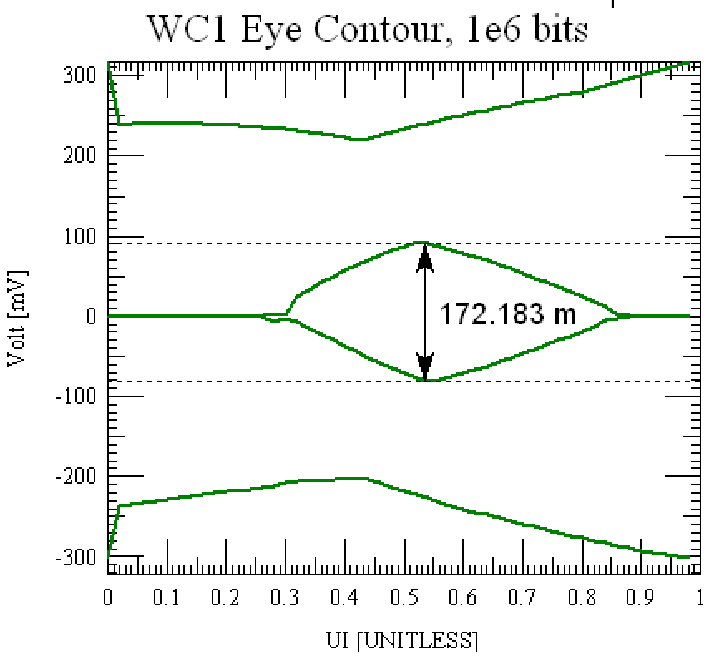
Step 6: Parameter Determination

#	Variable	Influences	Source	Value	Unit	Apply In	Notes
1	Tx Swing	Eye shape	SAS Spec Table 61	800	mV ppd	Tx Model	minimum allowed
2	Tx De-emp	Eye shape	SAS Tables 64 65	-2	dB	Tx Model	Ref Tx value
3	Bit Pattern	Jitter, Eye	SAS Spec, etc	CJTPAT		CA Form	
4	Dj	Eye, B-tub	Tx Parameter	23.4	pS p-p	chsim.clm	= 0.14% UI
5	Rotator Linearity	Eye, Bathtub	AMI Model Kit	pr_slow.dat	file	Rx model	pr_fast.dat a bit better
6	On-chip Sparams	Eye shape	AMI Model Kit	0		Tx/Rx models	enabled
7	Rj	Eye, B-tub	Tx Parameter	1.4	pS rms	CA Form	= 0.84% UI
8	Duty Cycle Dist.	Eye shape	Tx Parameter	0.05	UI	CA Form	Use 45 as HI%
9	Pj Magnitude	Jitter, Eye	AMI Model Kit	0.05	UI	CA Form	Enter as 0.05
10	Pj Cycles/UI	Jitter, Eye	AMI Model Kit	0.01	UI	CA Form	Enter as 0.01

- Extract from specs for worst-case analysis
- Unlike standard SI (has wc parameters in models)

Step 7: Corner Case Analysis

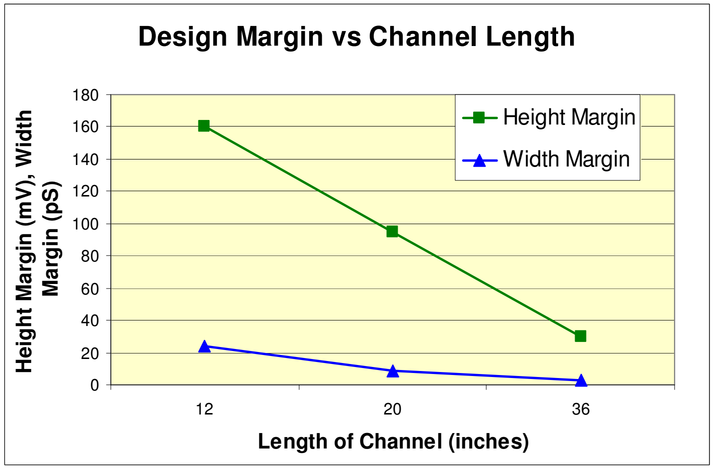




- Width: corner (red) decreases significantly to 0.25 UI
- Height: must derate to 1e15 (155 mV)
- Margin: 95mV/0.05UI against 60mV/0.20UI targets

Margins for All Systems

- Margins at 1e15 per SAS spec
- IBM Rx DFE Handles all Cases
- WC2 Margins Approaching Limit



Parameter	**TYP**	**WC1**	**WC2**	**Unit**
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# of Connectors	2	2	4	#
# of Vias	4	4	4	vias
Propagation Time	2.5	4	6	nS
6 Gbps bits in channel	15	24	36	bits
Channel Loss (SDD21 @ 3 GHz)	-8.9	-13.6	-16	dB
Crosstalk	9.1	5.6	7.4	mV rms
ISP	1.5	1.6	2.1	nS
#bits for Coverage	1e4	1e5	1e5	bits
Corner Eye Height (1e6 bits)	244	172	103	mV
Eye Height Margin (60 mV -10%)	**160**	**95**	**30**	mV
Typ Eye Width (1e6 bits)	0.72	0.59	0.52	UI
Corner Case Width (1e15 bits)	0.34	0.25	0.218	UI
Margin in UI (to 0.20UI target)	**0.14**	**0.05**	**0.018**	UI
Margin in pS	24	9	**3**	pS

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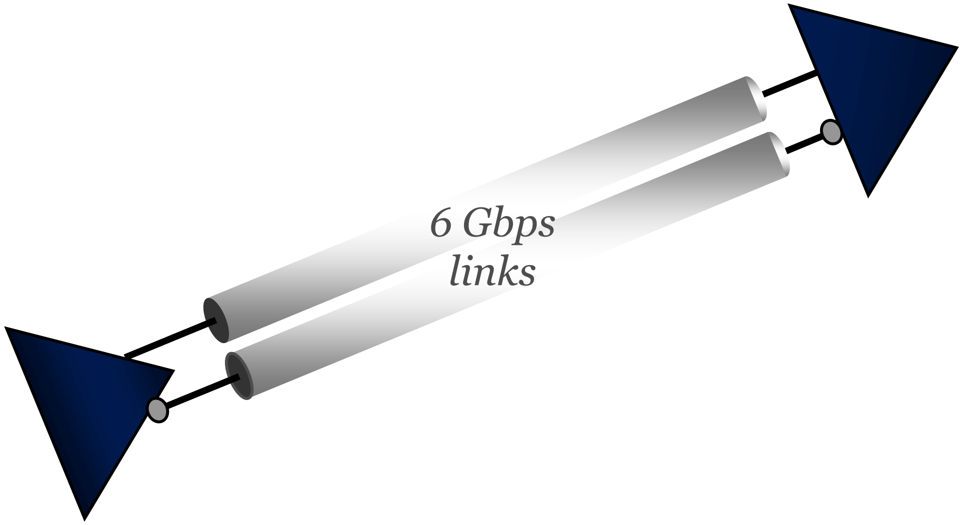
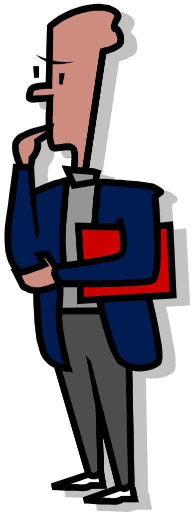


Key Learnings

- HDD implementation has margin against all tests, IBM SerDes performing well
- Worst-case margins become questionable around -16dB, typical channels <= -10dB
- 6 Gbps sim environment with AMI models now functional, performance meets expectations
- Environment enables compliance testing that previously required physical hardware

In Summary

- Serial link frequencies continue to increase
- Specs require virtual probing inside IC
- AMI models are starting to appear
- Simulation environment functional
- A process for link SI described
- Refer to paper for complete details



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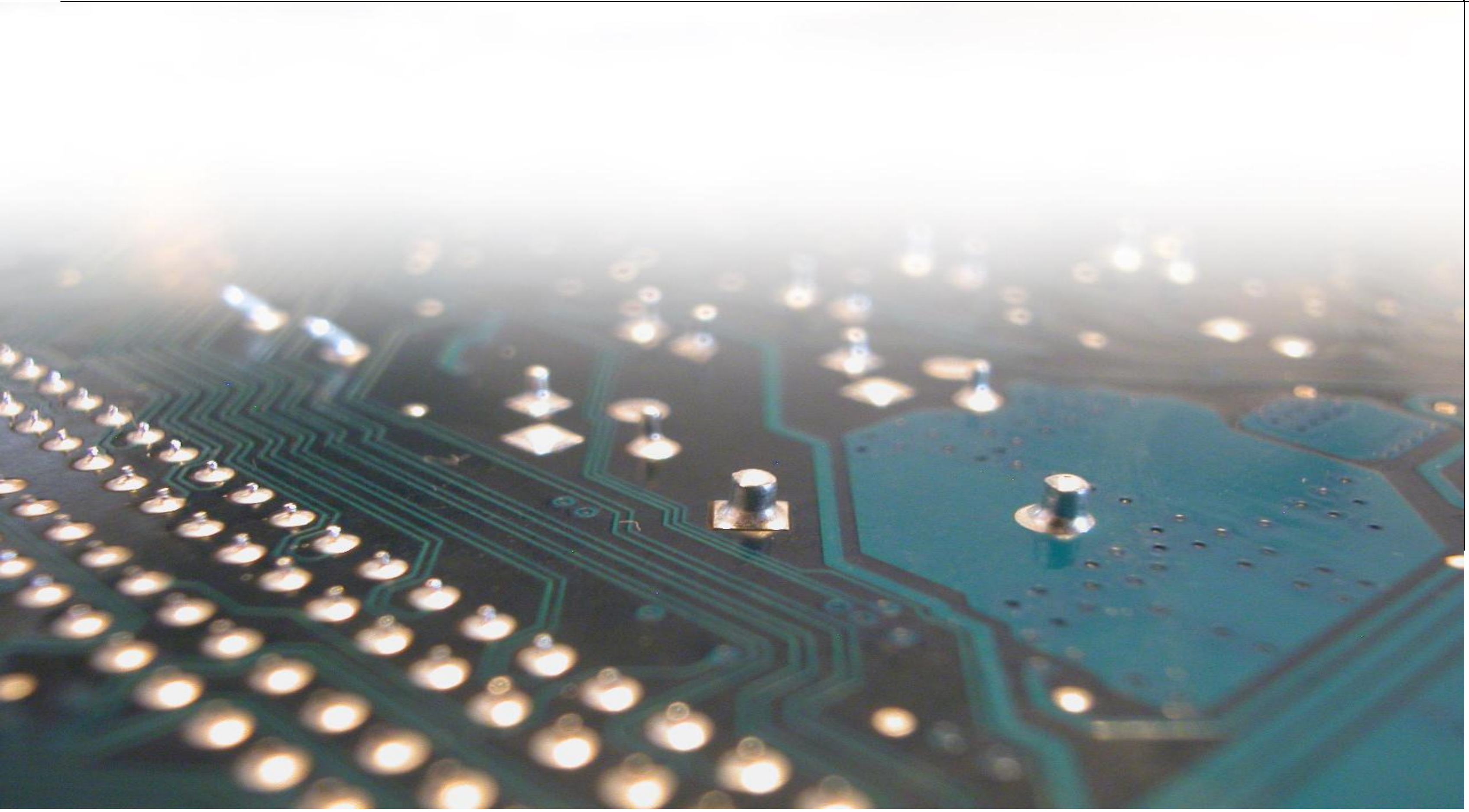

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