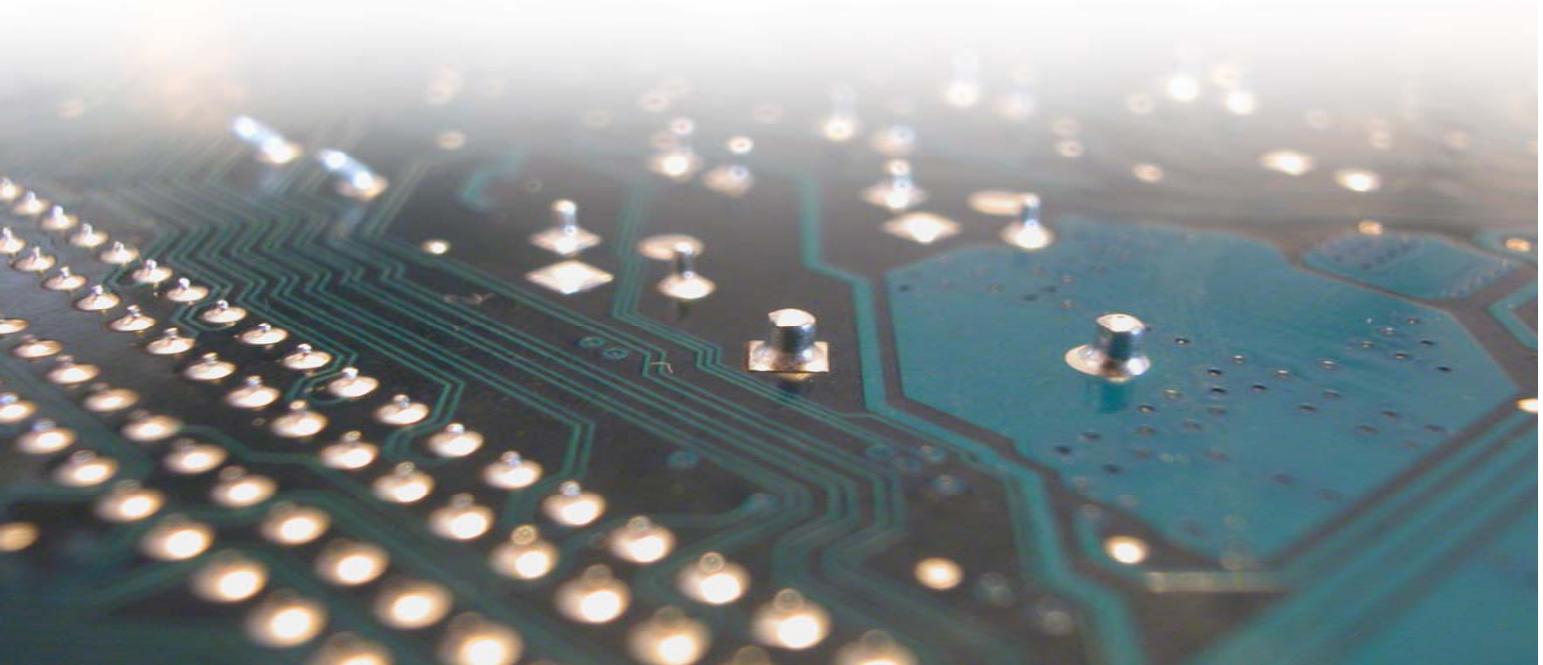
Using Allegro PCB SI GXL to Make Your Multi-GHz Serial Link Work Right Out of the Box

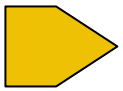
Session 8.11

Donald Telian - SI Consultant
Hamid Kharrati - A2e Technologies



A2e Technologies
Designing applications to electronics

Agenda

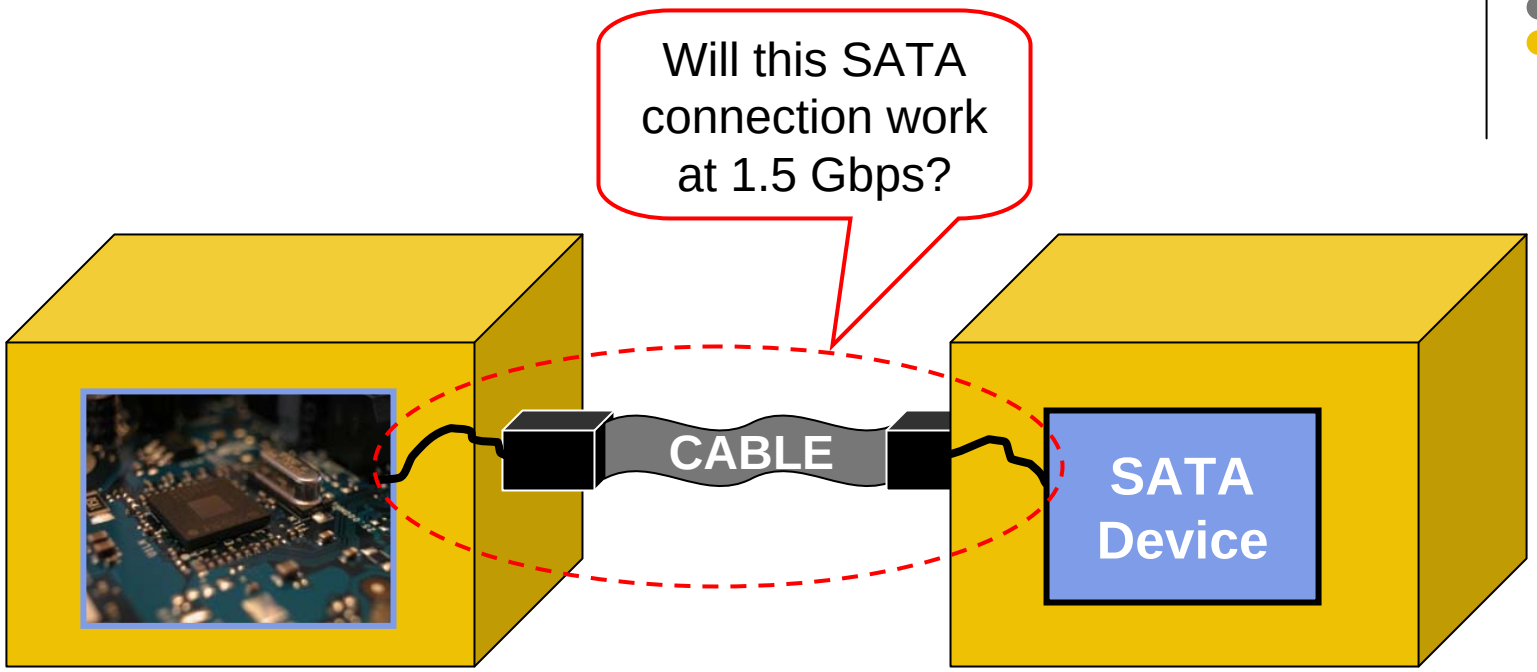


- About the Project
- Modeling the System
- Frequency Domain Analysis
- Signal Integrity Analysis
- Interpreting Results

Donald Telian
SI Consultant

A2e Technologies

Product Requirements



- Out of the box implementation
- Off-the-shelf SATA device at far end
- Signals traverse combination of cables & connectors
- Non-standard SATA MGH Serial Link

Donald Telian
SI Consultant

A2e Technologies

More Project Details

- Interconnect = 4 Connectors, 3 Cables

- Heavy-duty Bulkhead Connectors
- Far-end Device Undetermined
- Cables Undetermined
- PCB Routed (first rev.)

Donald Telian
SI Consultant

A2e Technologies

Topics Illustrated

- Process for MGH Serial Link SI
- How to Model an MGH System
- Value of Spec-level MacroModels
- The Problem with Stubs
- Pros/Cons of VNA Characterization
- Verifying Adherence to Specs

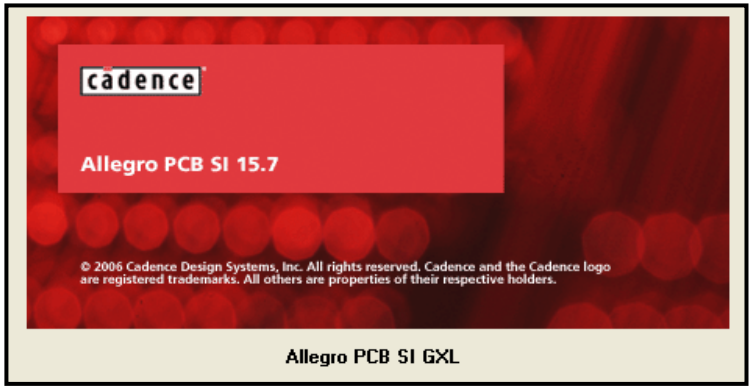
More detail in the paper!

Donald Telian
SI Consultant

A2e Technologies

Allegro SI GXL Features

- Time & Frequency Domain Analysis
- Differential-Pair Extraction
- SerDes Macromodels
- SigXp as Sandbox
- Channel Analysis
- S-Parameters
- Eye Diagrams



Donald Telian
SI Consultant

A2e Technologies

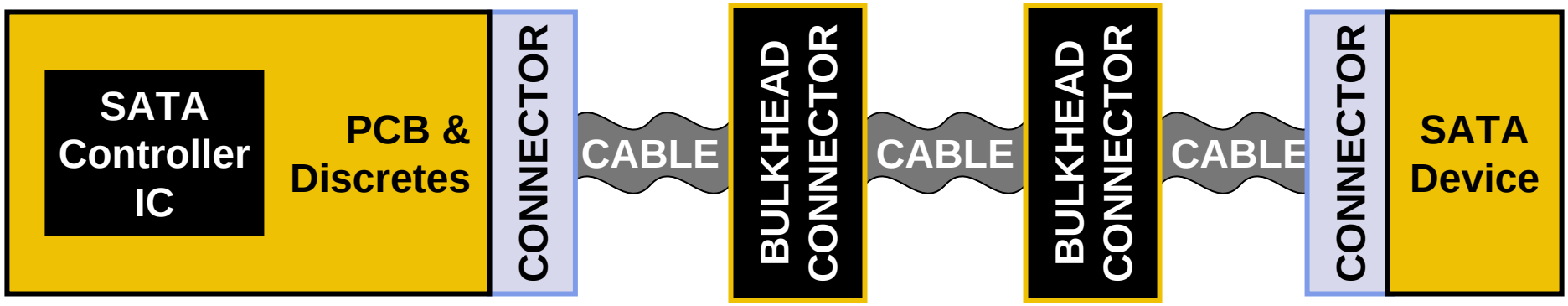
Agenda

- About the Project
- Modeling the System
- Frequency Domain Analysis
- Signal Integrity Analysis
- Interpreting Results

Donald Telian
SI Consultant

A2e Technologies

Components to Model



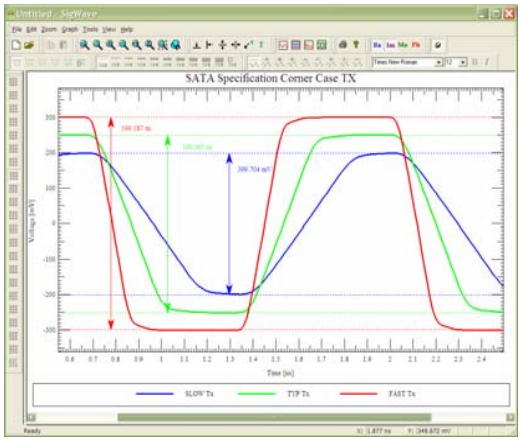
- Tx and Rx
- PCB & Discretes
- Cables & Connectors
- End-to-End System

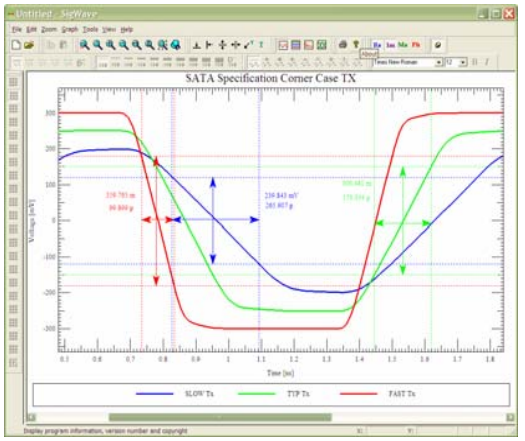
Donald Telian
SI Consultant

A2e Technologies

Tx and Rx MacroModels (F/T/S)

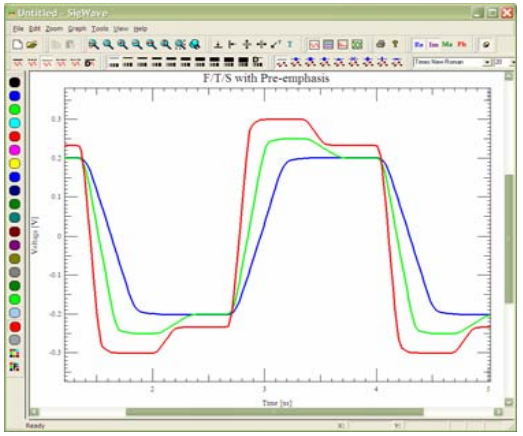
SATA Spec Voltage Swing & Edge Rates

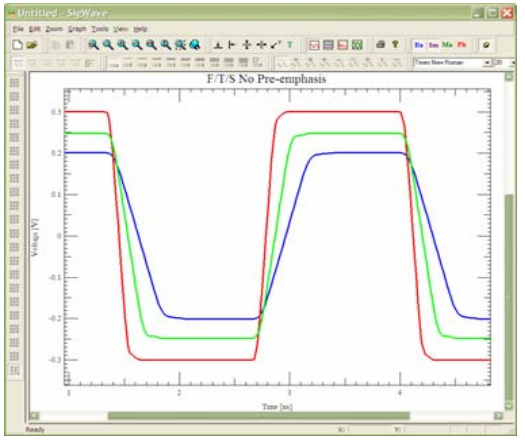




SATA Device

One set with 10% pre-emphasis, one set without (not in spec)





SATA Controller IC

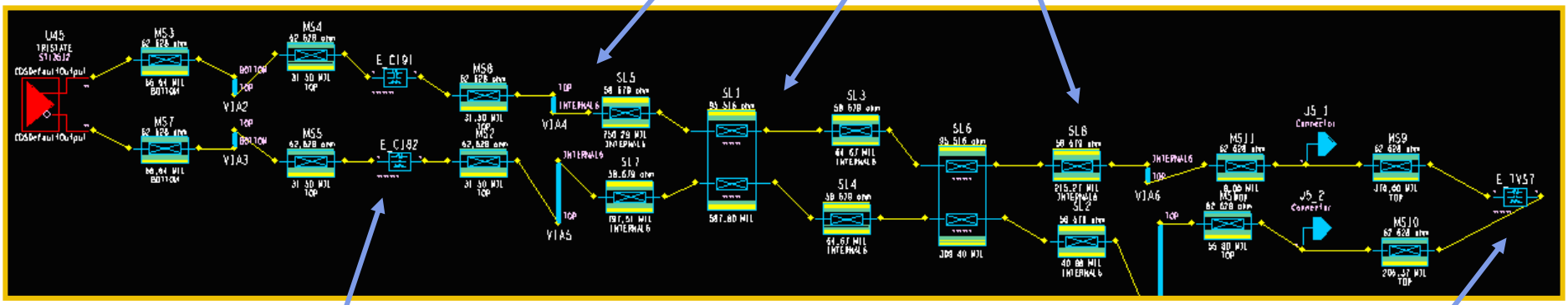
- Spec-corner models bound potential devices at other end
- Model also covers for controller IC's nonexistent or late model

Donald Telian
SI Consultant

A2e Technologies

PCB & Discrete Models

Etch, diff-pairs, vias extracted from PCB stackup



Series Capacitors include only ESR & ESL

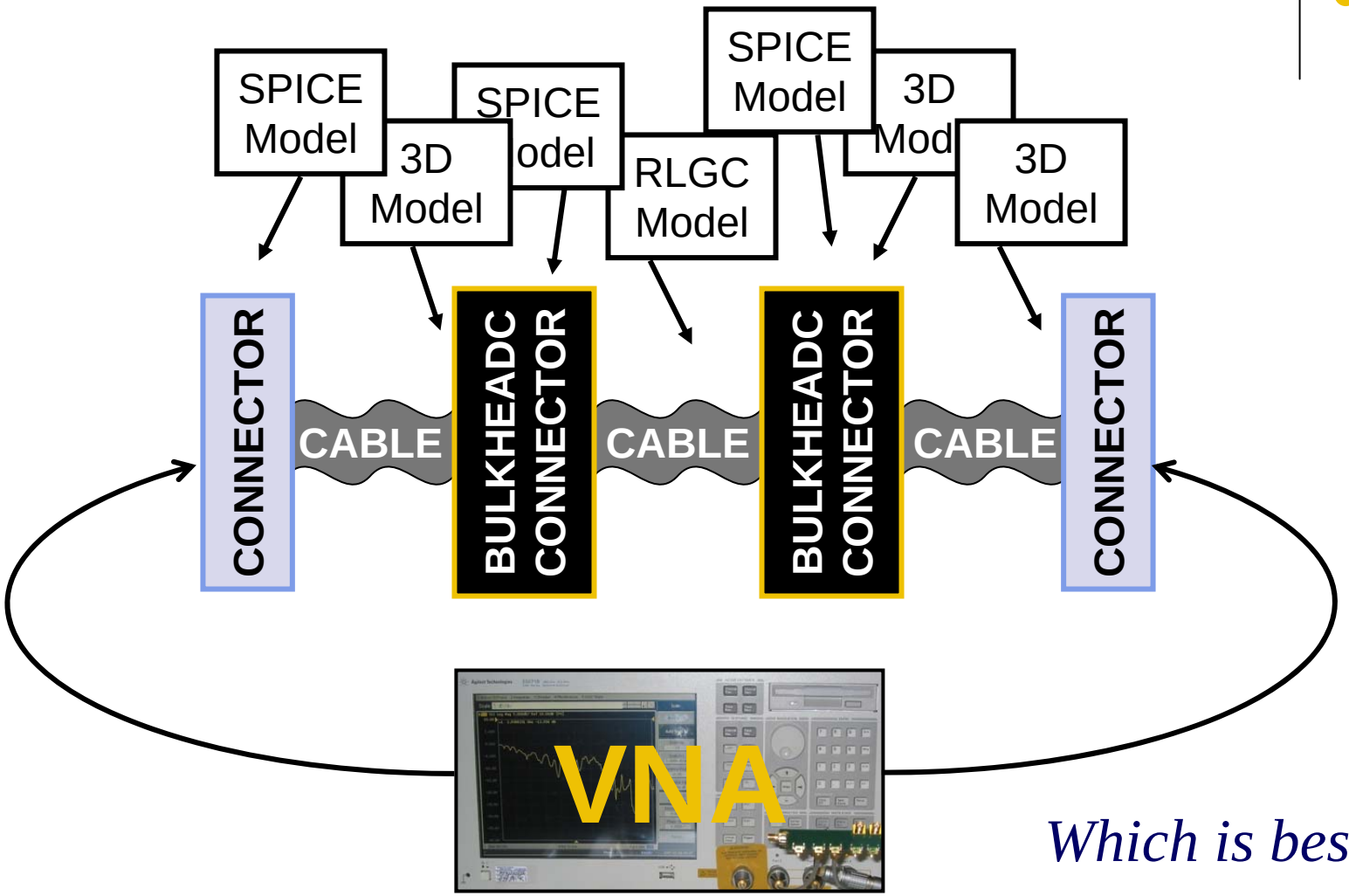
Via models can be regenerated in various formats

ESD Device modeled in Espice per datasheet

Donald Telian
SI Consultant

Technologies

Cable & Connector Options

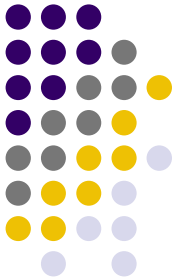


Which is best?

Donald Telian
SI Consultant

A2e Technologies

Which Option is Best?



VNA S-Parameters

- Need prototype
- Difficult to fixture
- End-to-end model
- Auto-correlation
- Hard to tolerance

Use for long, complex, cascaded configuration

3D Model Creation

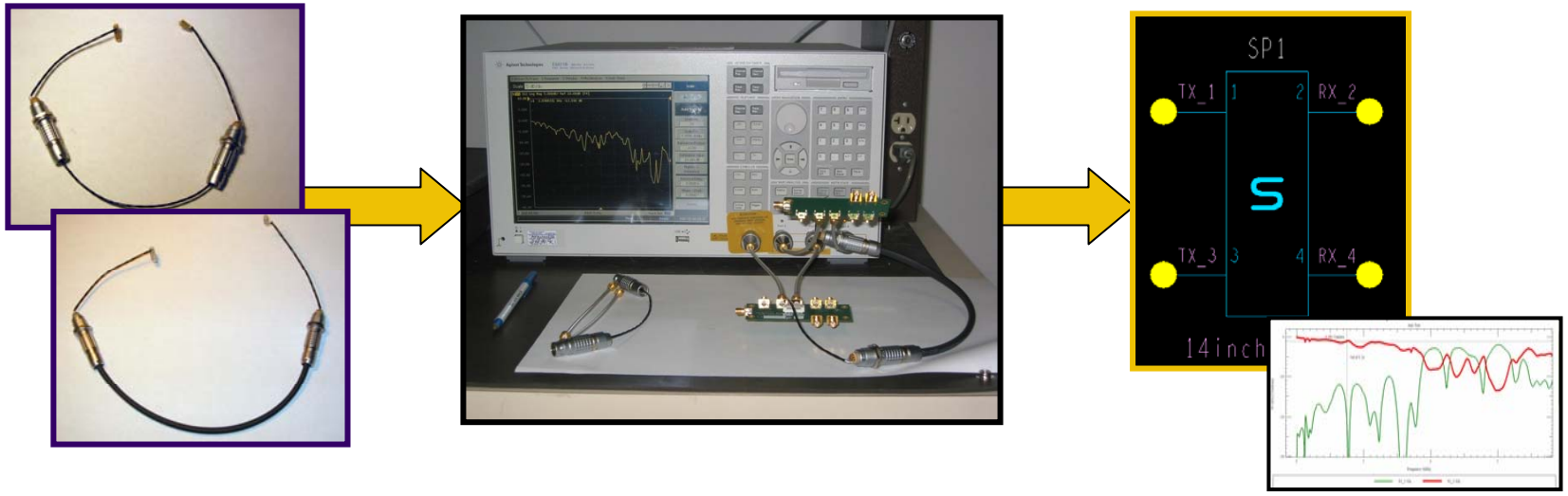
- Need drawings & mat'ls
- Lots of models
- Cascaded model
- Accuracy less clear
- Best/worst case

Use for single elements with importable drawings

Donald Telian
SI Consultant

A2e Technologies

VNA S-Parameter Model

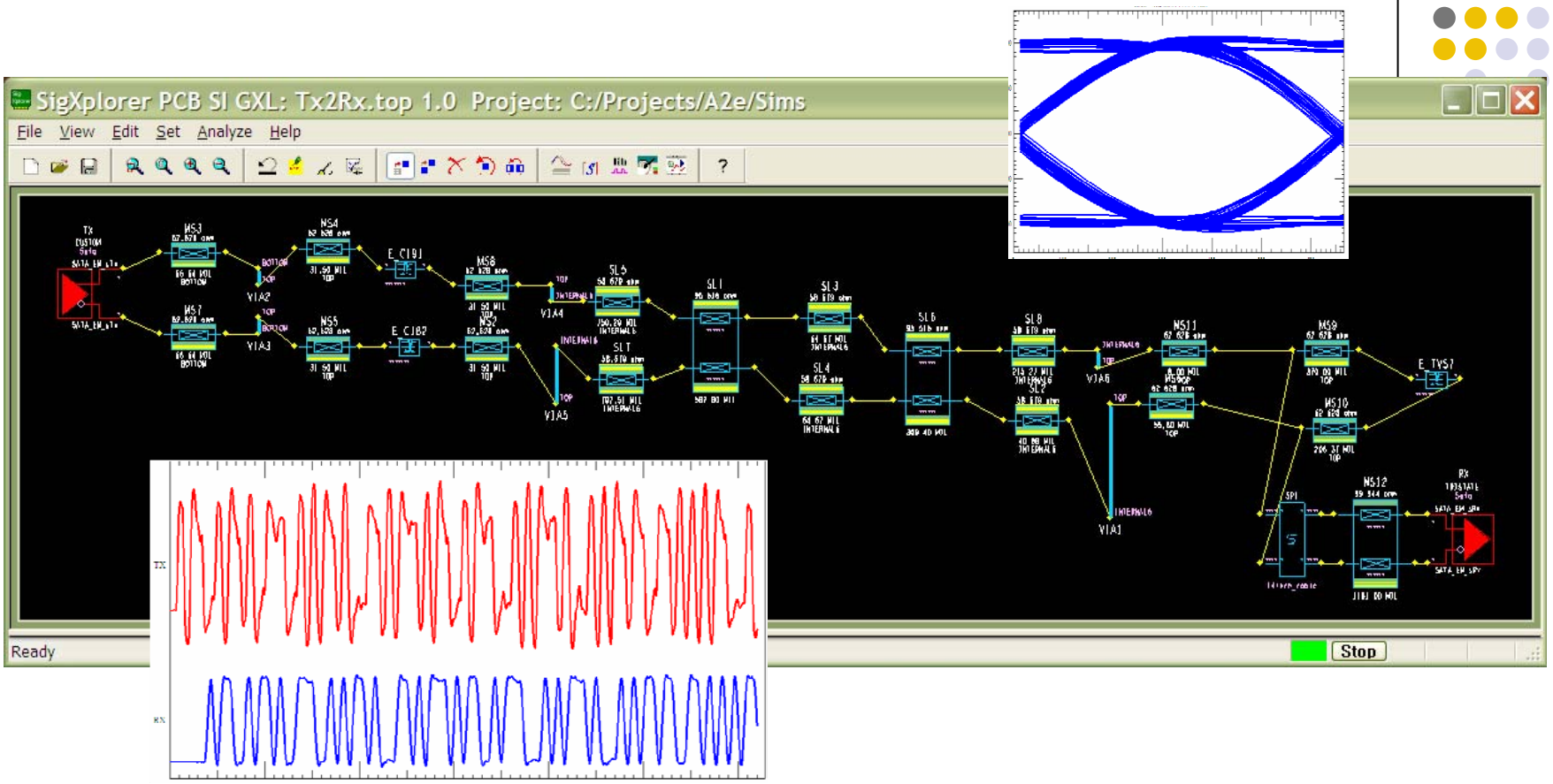


- 2 prototypes built/measured, Touchstone file output
- Simple PCBs were built for 4-port measurement
  - SMA connectors, calibration structures (open, short, load)
  - Direct soldering of coax unstable and inefficient

Donald Telian
SI Consultant

A2e Technologies

Putting it all Together



- All pieces assembled in SigXp
- Waveforms show models perform as expected

Donald Telian
SI Consultant

A2e Technologies

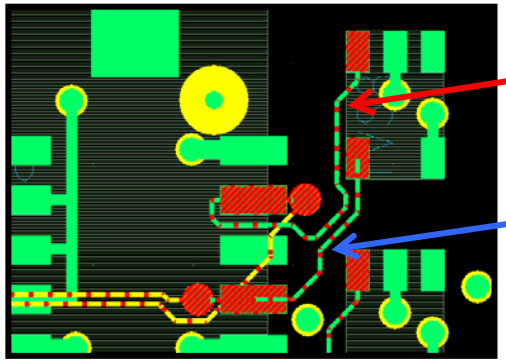
Agenda

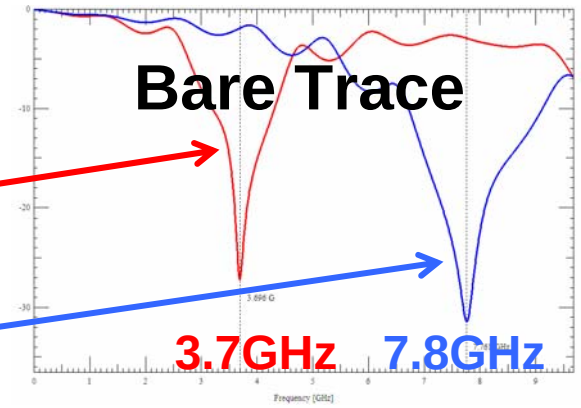
- About the Project
- Modeling the System
- Frequency Domain Analysis
- Signal Integrity Analysis
- Interpreting Results

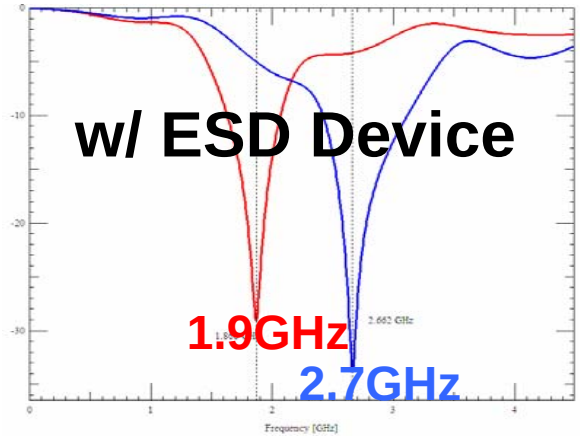
Donald Telian
SI Consultant

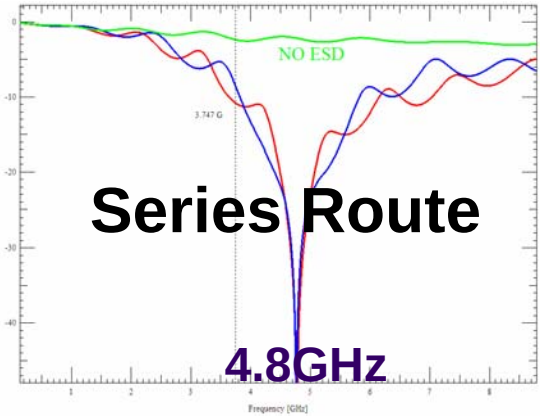
A2e Technologies

Frequency Domain Analysis









Problematic_Stub_Length
= (¼) * (Vel_pcb/freq)
= (¼) * (5.9 in/ns / freq)
= **400** or **190** mils

- Stubs to ESD devices problematic
  - -30 dB at noted frequencies
- SI improves 7% if routed in series

Donald Telian
SI Consultant

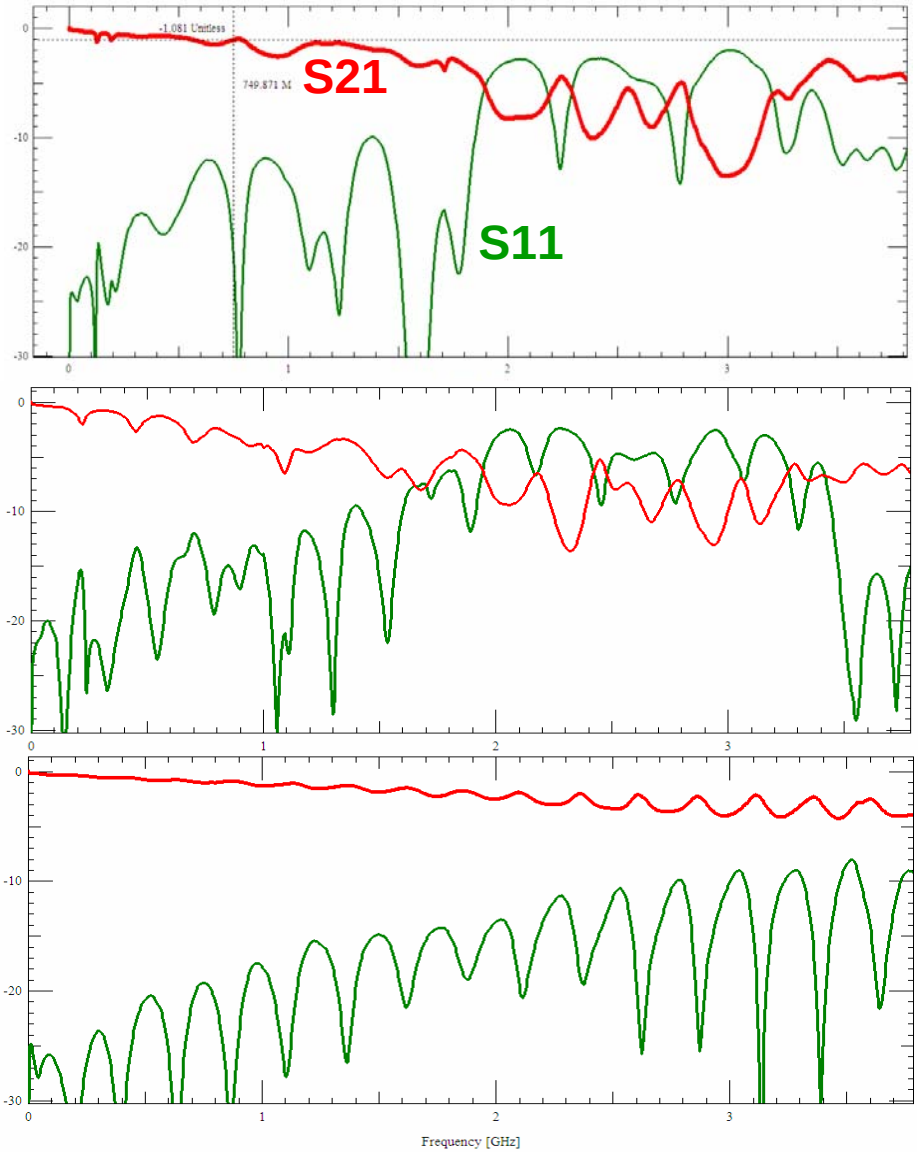
A2e Technologies

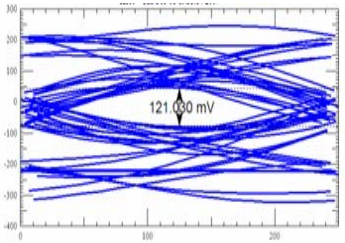
VNA Plots

Cable 1

Cable 2

No Bulkhead





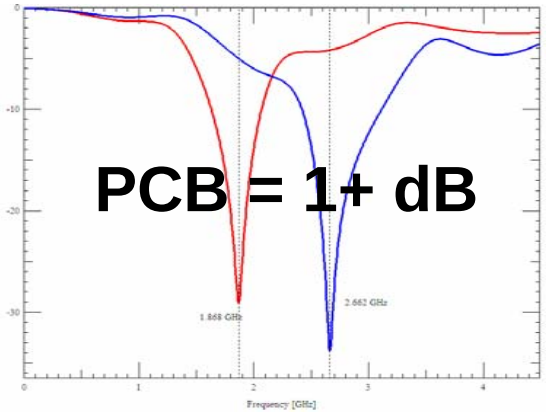
Gen2 SATA not likely!

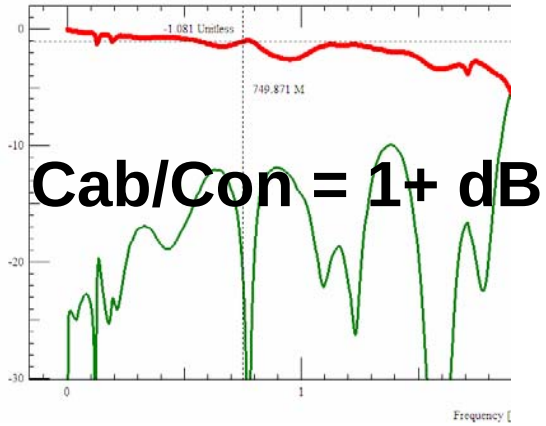
Bulkhead connector causes more reflection than transmission (S11 > S21) from ~1.5 to 3 GHz

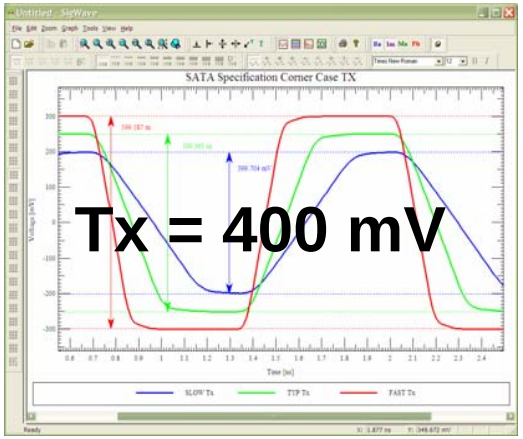
Donald Telian
SI Consultant

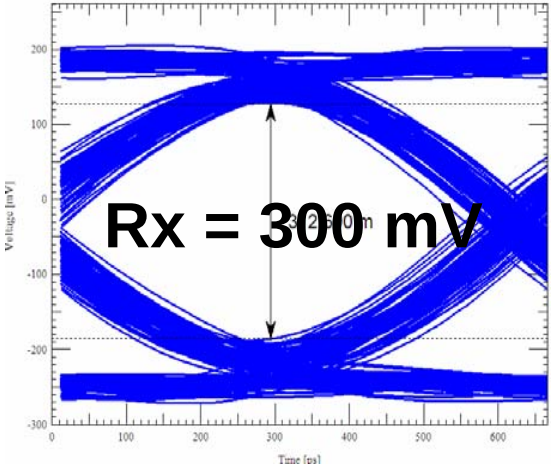
A2e Technologies

Loss Budgets at 1.5 Gbps









Summed budget of about 2.5 dB implies 25% (=1 – 10^[dB/20]) of signal will be lost from Tx to Rx

As expected, 400mV at Tx becomes about 300 mV at Rx

Donald Telian
SI Consultant

A2e Technologies

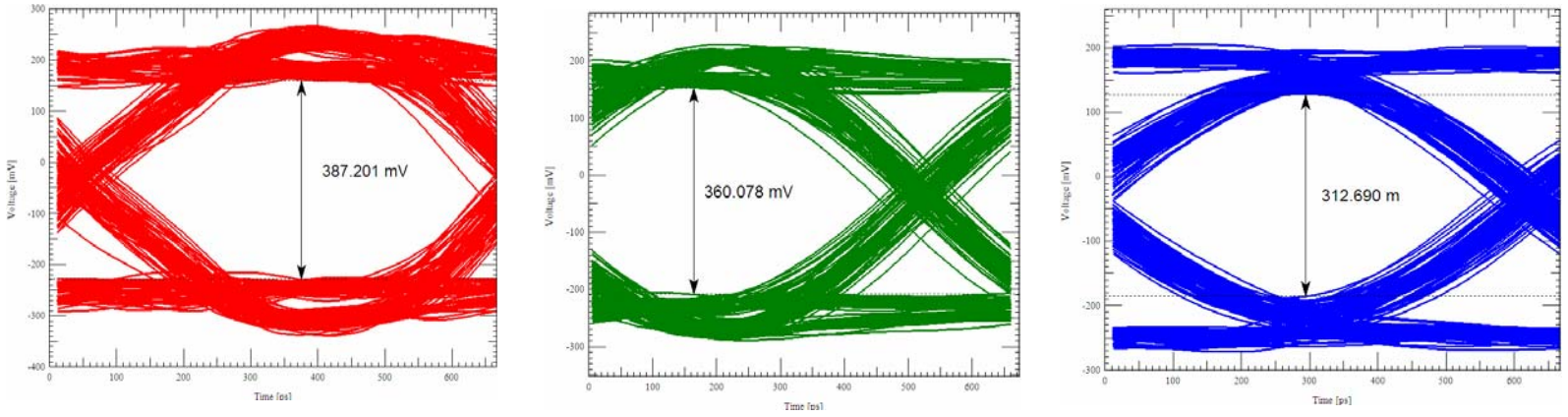
Agenda

- About the Project
- Modeling the System
- Frequency Domain Analysis
- Signal Integrity Analysis
- Interpreting Results

Donald Telian
SI Consultant

A2e Technologies

Fast/Typ/Slow Eye Diagrams

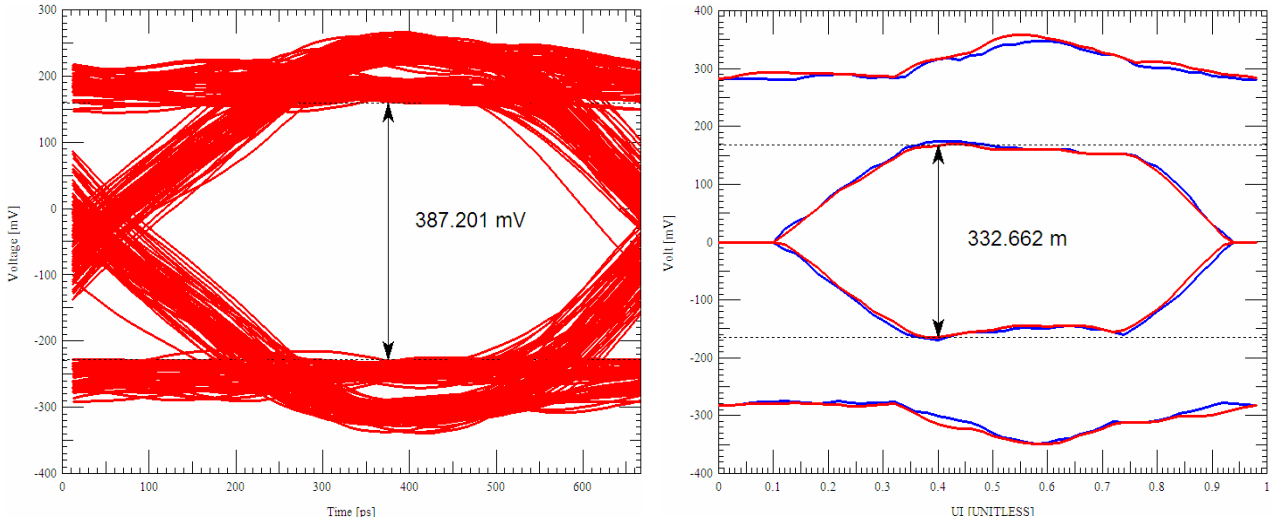


- SATA Gen1i min spec is 325 mV, Gen1m is 240 mV
- F/T/S measure 387/360/**313** mV, respectively
  - Slight violation of Gen1i spec at slow corner
- Fast corner ringing prompts longer bit stream test

Donald Telian
SI Consultant

A2e Technologies

Channel Analysis



- 250 bits compared to 10,000 and 1,000,000 bits
  - Note similar shape of eye contour
- Ringing on Fast corner causes 55 mV collapse
- Rx may not see this (reads real-time bit stream)
- Typ and Slow corners do not exhibit this behavior

Donald Telian
SI Consultant

A2e Technologies

About Jitter

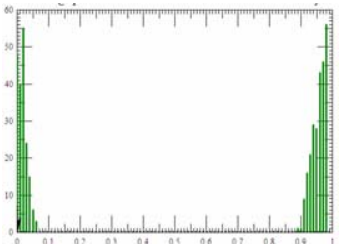
- Spec simplifies handling of Rj
  - There are two types of jitter, random jitter (RJ) and deterministic jitter (DJ). Random jitter is Gaussian and unbounded. For ease, the standard deviation (RJ_σ) is multiplied by a factor which corresponds to the target BER. For a target BER = 10^{-12}, the associated multiplication factor for Serial ATA is 14.

    Total jitter (TJ) is peak-to-peak and defined as:

    $$TJ = (14 * RJ_\sigma) + DJ$$

  - as such, enter 14*Rj directly into tool
  - component datasheets specify Rj

- Spec allows generous Tj of 0.6*UI at Rx
- System found to be stable
  - good jitter margin



Donald Telian
SI Consultant

A2e Technologies

SI Results

SI RESULTS			SIMULATED			MARGIN		
Parameter	**spec**	**units**	**min**	**typ**	**max**	**min**	**typ**	**max**
CABLE 1								
Gen1i Eye	325	mV min	312	360	333	**-13**	35	8
Gen1m Eye	240	mV min	"	"	"	72	120	93
Dj	0.35	UI max		0.16			0.19	
Tj	0.6	UI max		0.22			0.38	
CABLE 2								
Gen1i Eye	325	mV min	305	345	306	**-20**	20	**-19**
Gen1m Eye	240	mV min	“	“	“	65	105	66
Dj	0.35	UI max		0.18			0.17	
Tj	0.6	UI max		0.23			0.37	

- Two cable options tested
- Generous jitter specs, non-issue
- Slight eye height margin violations

Donald Telian
SI Consultant

A2e Technologies

Agenda

- About the Project
- Modeling the System
- Frequency Domain Analysis
- Signal Integrity Analysis
- Interpreting Results

Donald Telian
SI Consultant

A2e Technologies

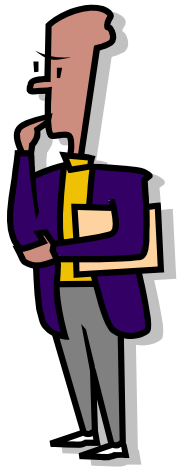
Interpreting Results

- System works well, assuming
  - Devices at far end are Gen1m compliant
  - Routing changes are made (7% more margin)
- More margin in “Specsmanship”
  - SATA spec’s values at “connector”
  - Not clear actual devices adhere to this
- System likely not upgradeable to 3 Gbps Gen2
  - Bulkhead connectors an issue
  - More analysis necessary

Donald Telian
SI Consultant

Problems & Learnings

- S-Parameters are great, but new
  - Accurate measurement is challenging
  - Not all simulators handle them the same
- Pre-emphasis is not always good
  - At 1.5 Gbps, it can work against you
  - Ability to simulate the options is helpful
- Mechanicals must bend to Multi-GHz rates
  - Be sure to double-check desired interconnect
  - Need to update routing practices



Donald Telian
SI Consultant

In Conclusion

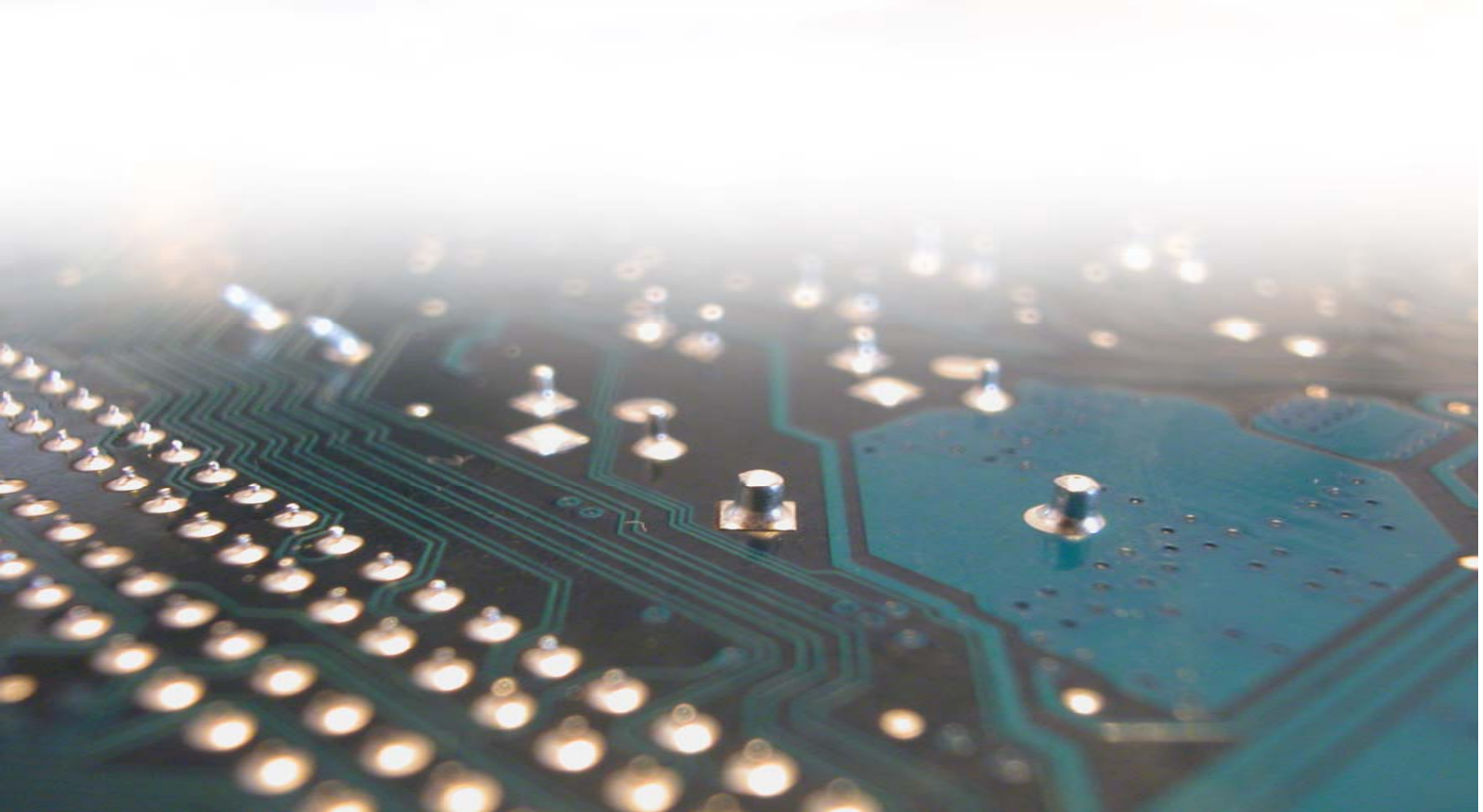
- Illustrated a serial link design process
- Highlighted MGH modeling shortcuts
- Described how to apply Allegro PCB SI
- Explained new tools and techniques

…to help your design work right out of the box

Donald Telian
SI Consultant

A2e Technologies

THANK YOU



cadence™

cadence designer network

cdn LIVE™

CONNECT: IDEAS

CDNLive! 2007 Silicon Valley