New Techniques for Designing and Analyzing Multi-GigaHertz Serial Links

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Agenda

1. Wide Eyes and More Bits
2. Interconnect Storage Potential (ISP)
3. Channel Analysis
4. PCI Express Case Study
5. Serial ATA Case Study
6. Summary & Conclusions

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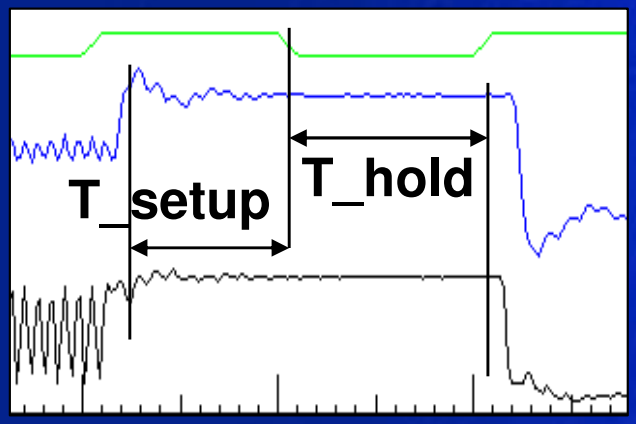
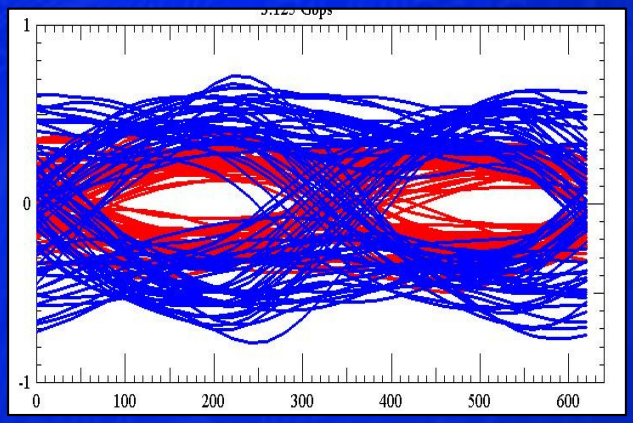
Serial Links: Changes and Challenges

- Embedded Clocks
- Eye Diagrams

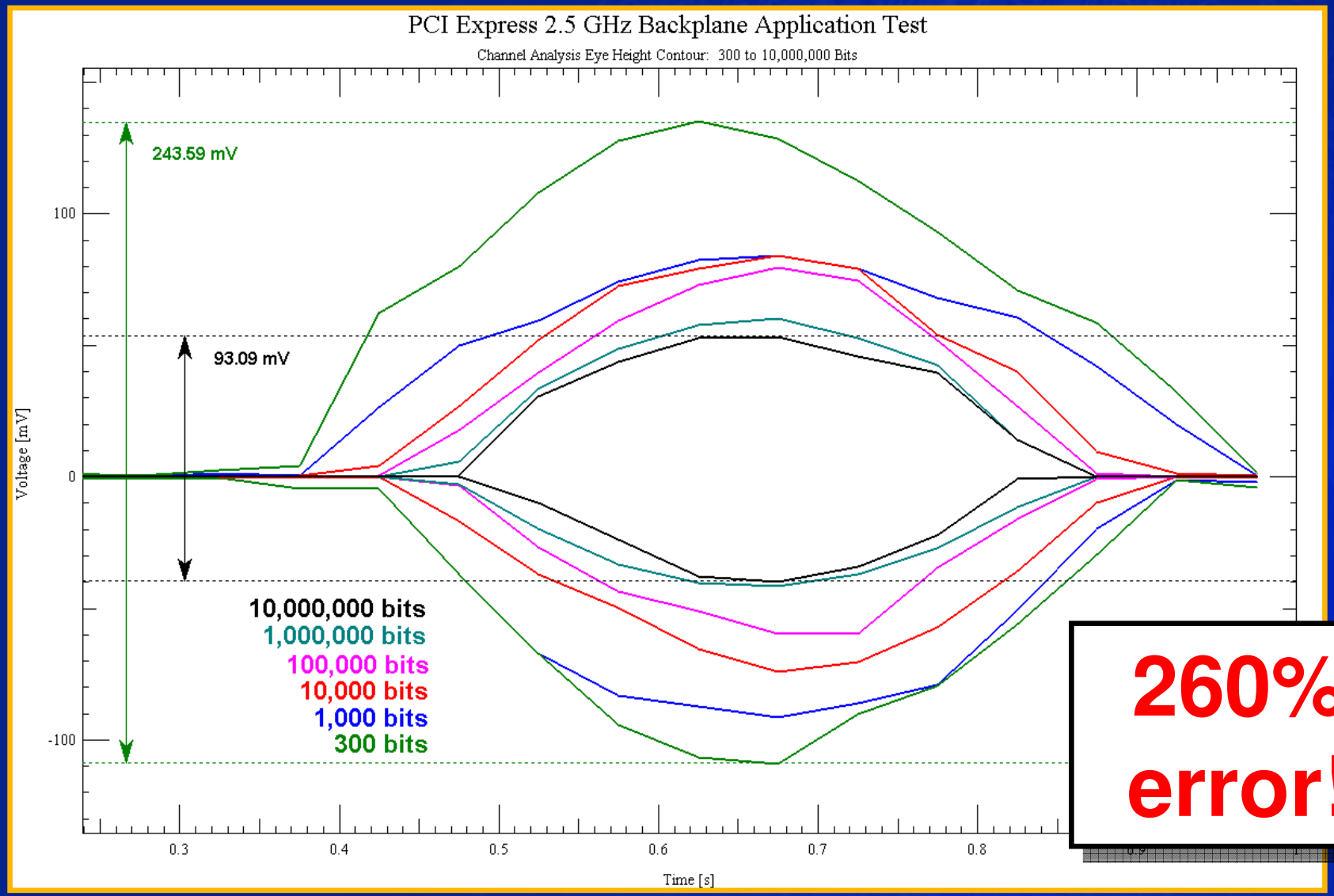


single cycle



many cycles

But how many cycles?



260% error!

Do all links do that?

- No
  - but it sure helps to find the ones that do!

How can you find them?

  - understand and quantify the link's Interconnect Storage Potential, or "ISP"

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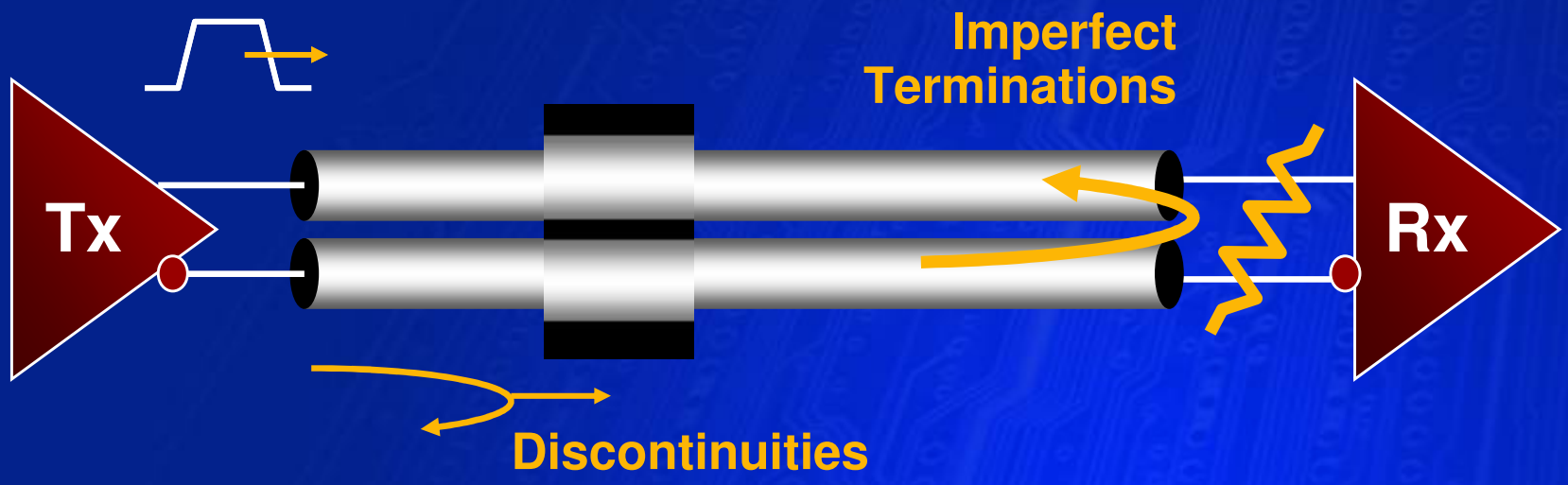
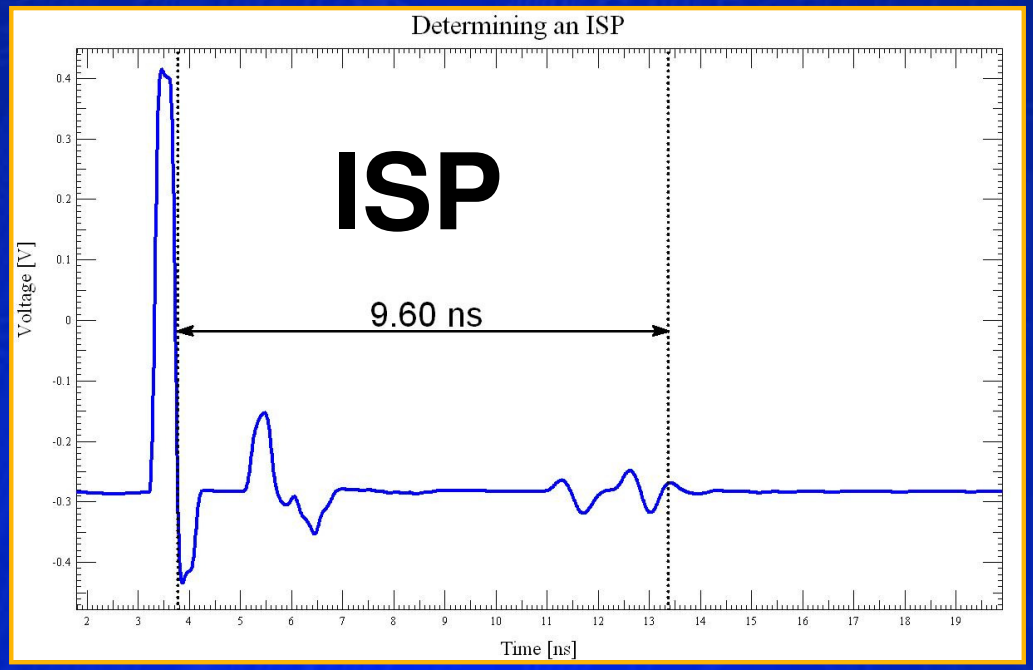
Interconnect Storage



- All links must store a signal
  - signals typically arrive at Rx 10 bit times after leaving Tx
- Unwanted energy often gets stored too
  - this interferes with the SI of later bits (ISI)

Interconnect Storage Potential

- Unique for each interconnect
- Measures how long a bit's energy stays in link
- Can be measured from pulse response
- Directly related to how many bits you need to simulate



Fingerprints an interconnect just like an I/V curve fingerprints a driver

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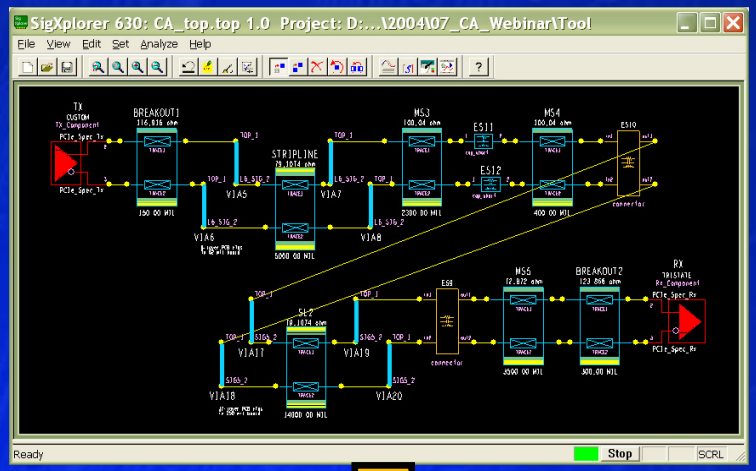
ISP-based Design Methodology

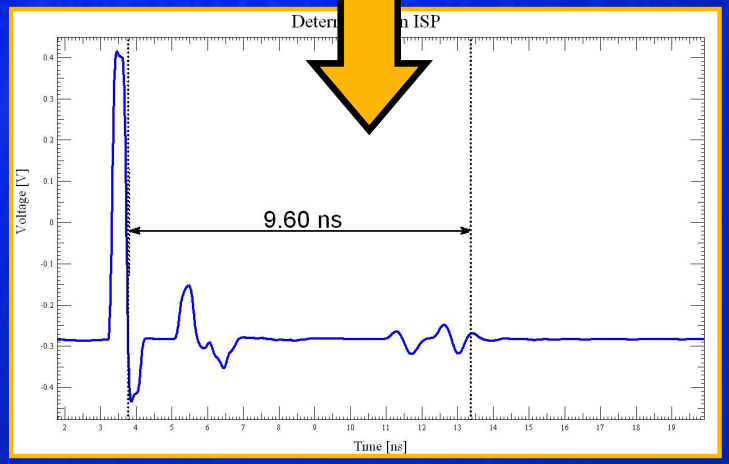
1. Determine the ISP
2. Determine the Relevant Preamble
3. Calculate the Number of Bits
4. Perform High-Capacity Simulation

We'll illustrate using both PCI Express and Serial ATA

1. Determine the ISP

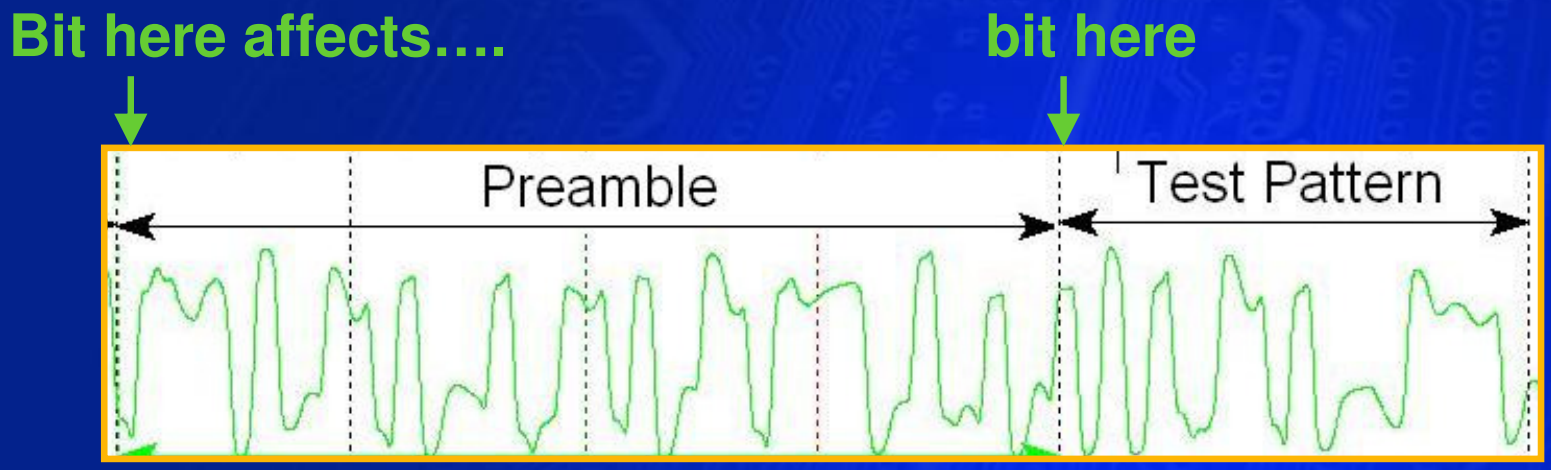
- Model
  - All effects
- Pulse
  - Bit time, or less
- Plot
  - Tx is best
- Measure
  - Fall to 5%, or
  - mV tolerance





2. Determine Relevant Preamble

Relevant if



Preamble = ISP / bit_time

In simple terms: how many bits fit in the ISP

3. Calculate Number of Bits

Number of unique patterns:

$$\#bits = (preamble) * 2^{(preamble)}$$

or

$$\#bits = (ISP*Gbps) * 2^{(ISP*Gbps)}$$

- Pessimistic due to overlapping
- Encoding schemes reduce further
  - 8b/10b removes power of 2 per 10 bits

4. High-Capacity Simulation

- Simulate #bits from step 3
  - For example, a 6 nS ISP on a 2.5 Gbps PCI Express link requires $(6*2.5) * 2^{(6*2.5)}$ bits, or ~500k bits
- SPICE simulation typically used on these links does ~ 100 bits/hour
  - would require over 200 days

Hmm… what good is a methodology like that !?

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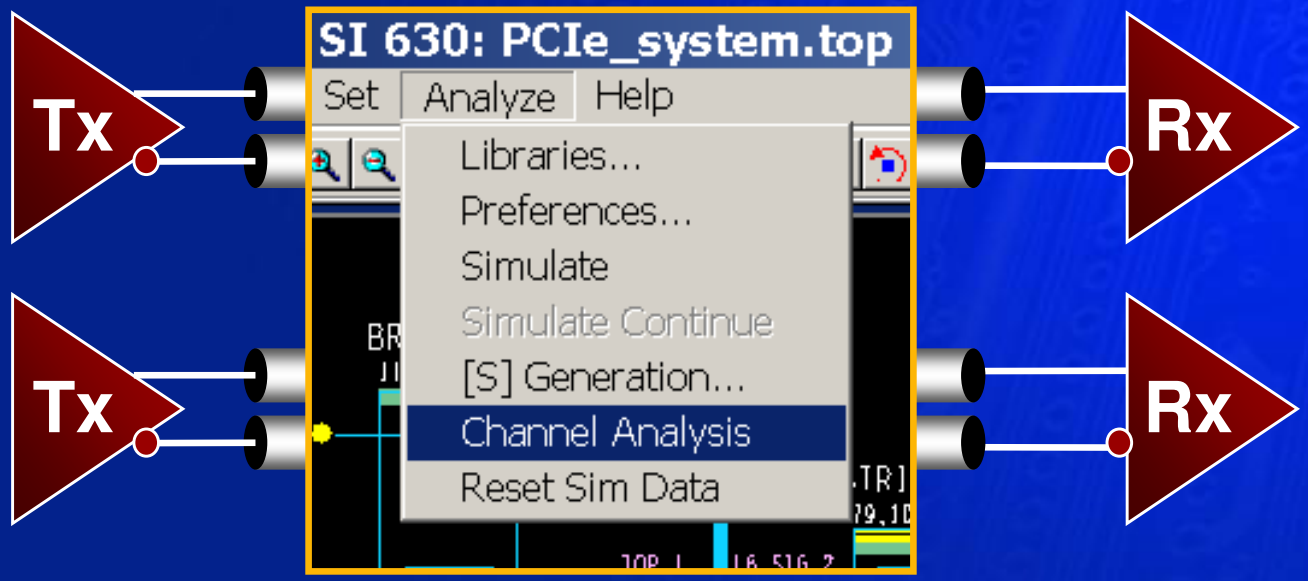
Introducing Channel Analysis

- New analysis capability in Allegro PCB SI
- FAST simulation of millions of bits
- Any differential topology, including pair-to-pair crosstalk
- Tx/Rx can be DML, MacroModel, IBIS, or Hspice
- Automatic PRBS, 8b/10b, random, or user-defined bits



NOT typical circuit simulation

How Fast Is Channel Analysis?

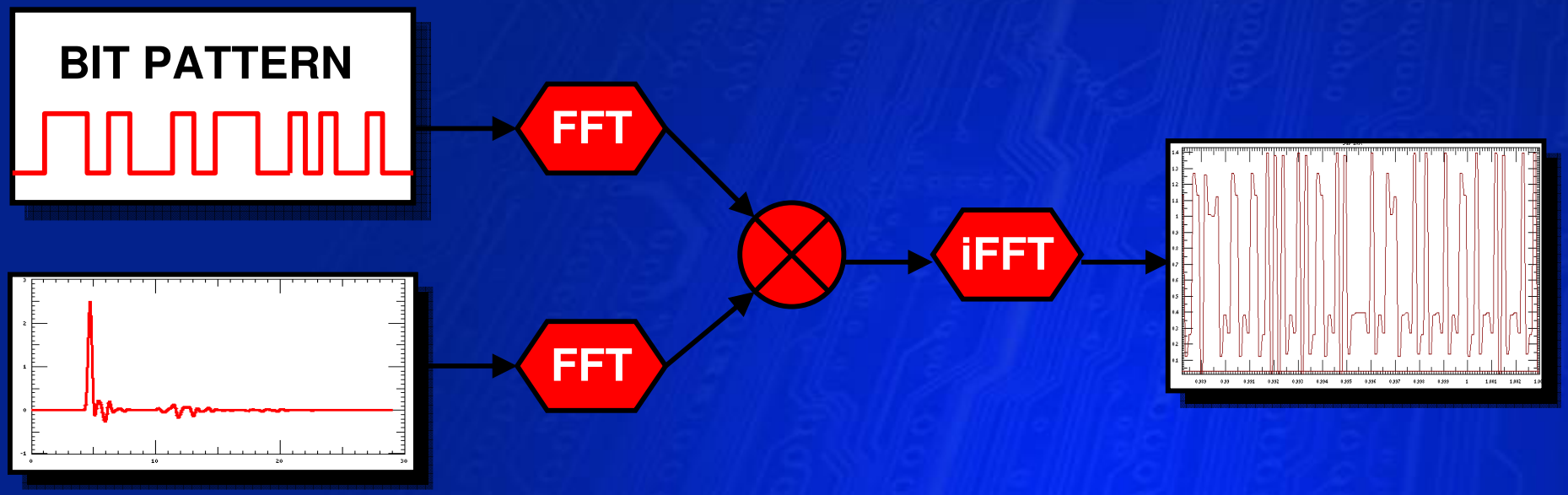
# bits	CA *	CA bits/sec	SPICE +	x faster
1,000	5 sec	200	10 hours	7,200
10,000	7 sec	1,400	4 days	51,000
100,000	20 sec	5,000	1.4 months	180,000
1,000,000	2.5 min	6,300	1 year	225,000
10,000,000	24.5 min	6,800	11 years	245,000

* PCI Express topology shown, IBM T41 laptop, Windows XP, 1.6 GHz Pentium M (proceeded by 7.5 min fingerprint “characterization”)

+ SPICE simulation time of 100 bits/hour (0.03 bit/sec) based on sample transistor-level SerDes model in a typical 3.125 Gbps channel

- More tool detail at: http://www.cadence.com/webinars/webinars.aspx?xml=channel_analysis
- Alternative worst case pattern methodologies referenced in paper, not considered faster or as robust

What Mathematical Method Does CA Use?



- Requires characterization of interconnect (its “fingerprint”)
- Techniques have been used in other disciplines for years
  - But new to digital PCB signal integrity

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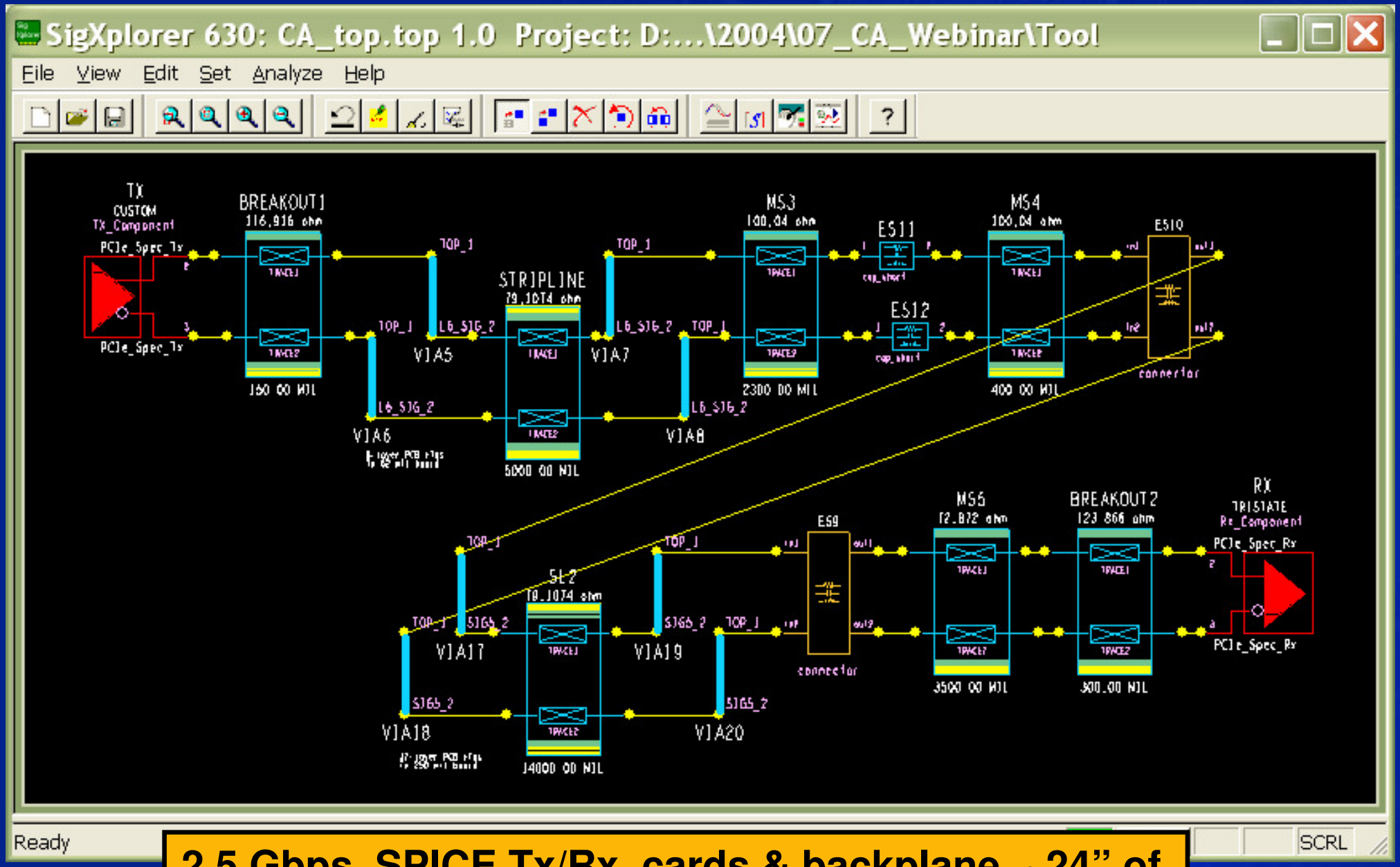
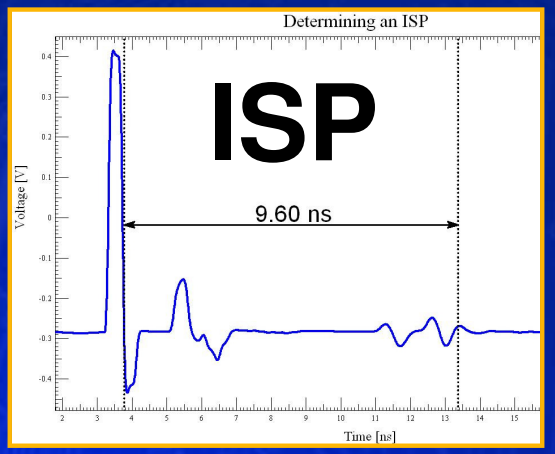
PCI Express Topology:



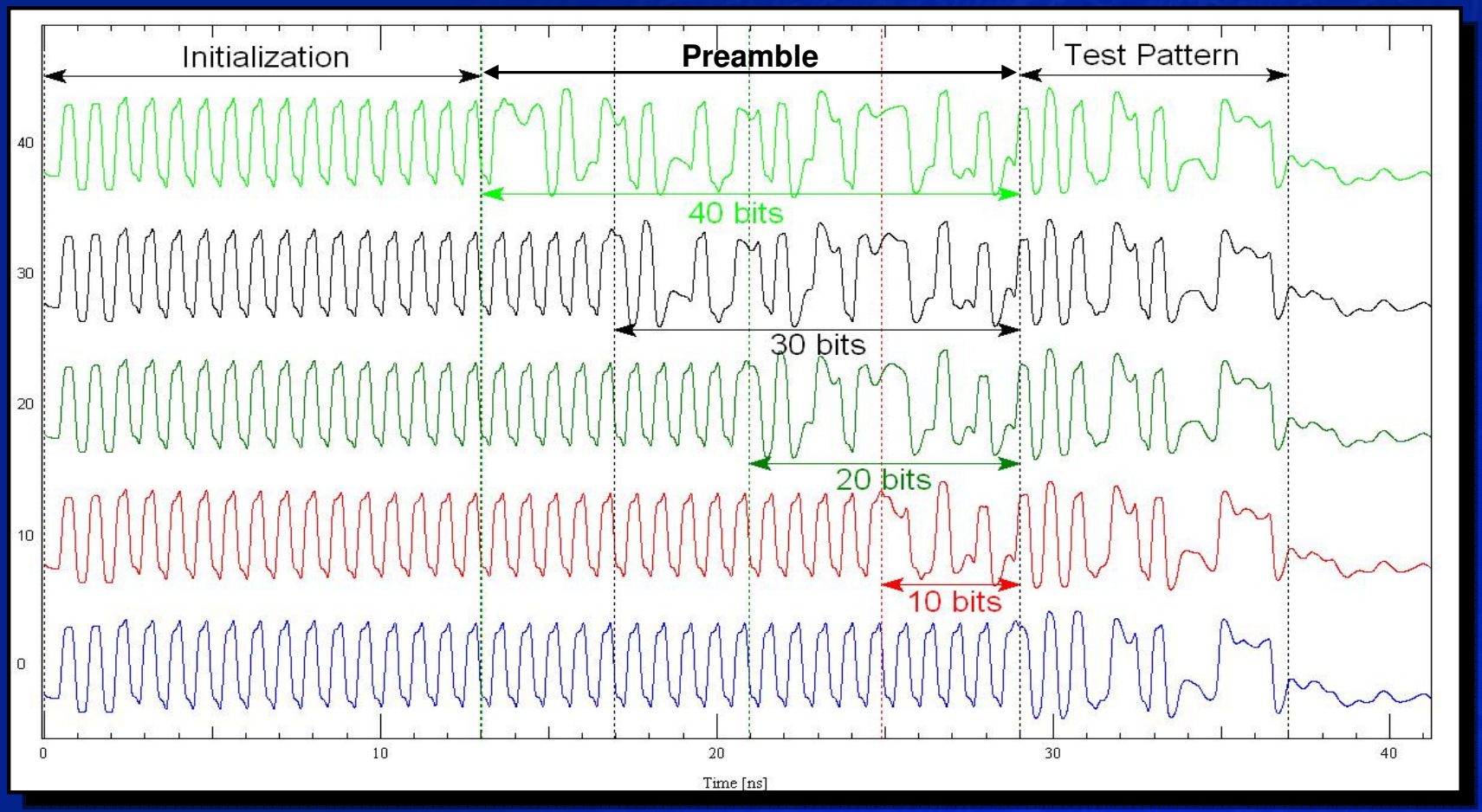
2.5 Gbps, SPICE Tx/Rx, cards & backplane, ~24” of trace, 2 connectors, 8- & 32-layer S-parameter vias

Methodology Steps



1. Determine the ISP
   - Simulation shows ISP = 9.6 nS
2. Determine Relevant Preamble
   - 2.5 Gbps Preamble = 9.6 nS / 400 pS = 24 bits
3. Calculate Number of Bits
   - For 8b/10b, #bits = 24×2^{22} ~= 100 million
4. Perform High-Capacity Simulation
   - Do Channel Analysis to see eye height

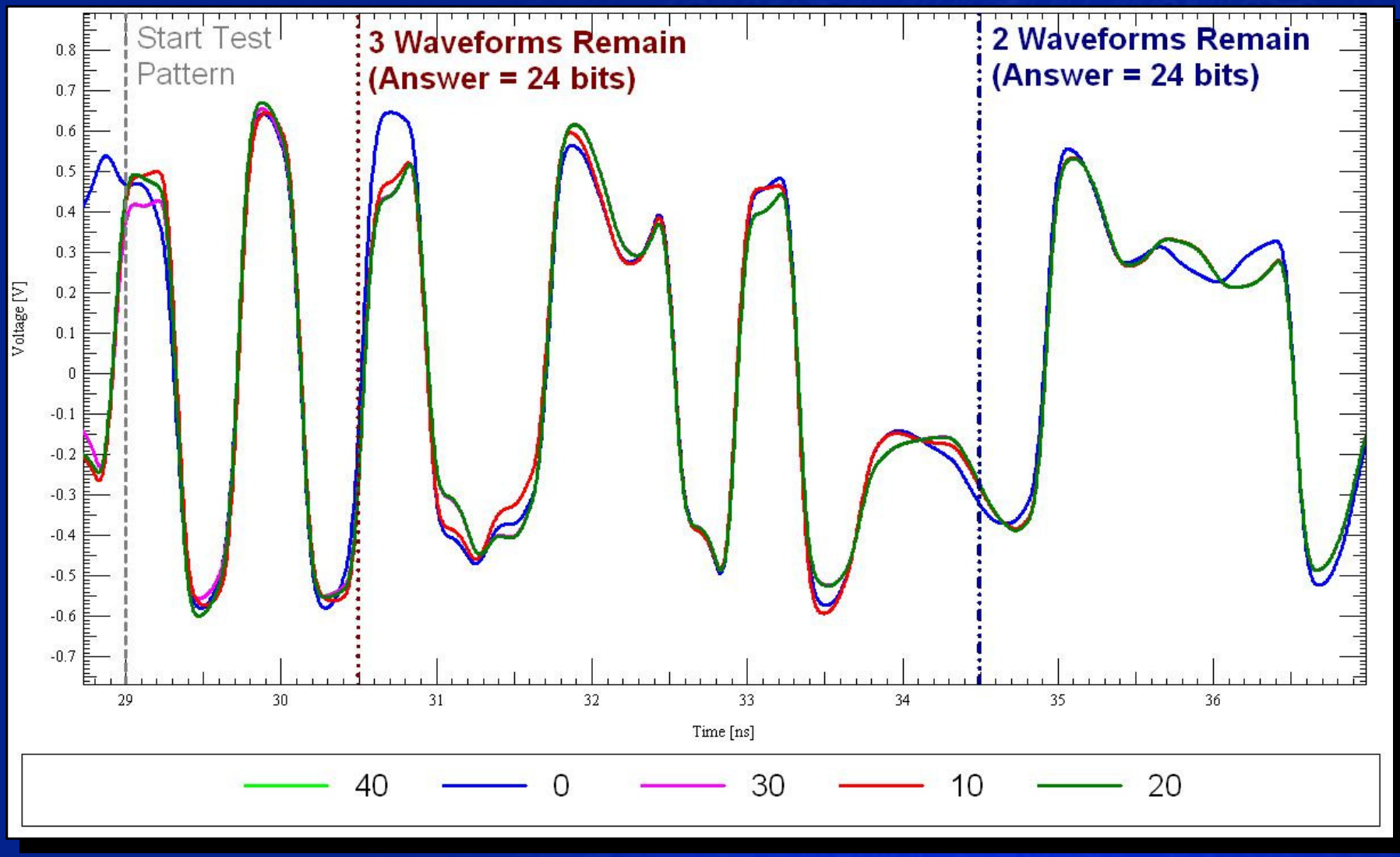
Verify Relevant Preamble



Constant Test Pattern, 1 to 4 8b/10b pattern Preamble

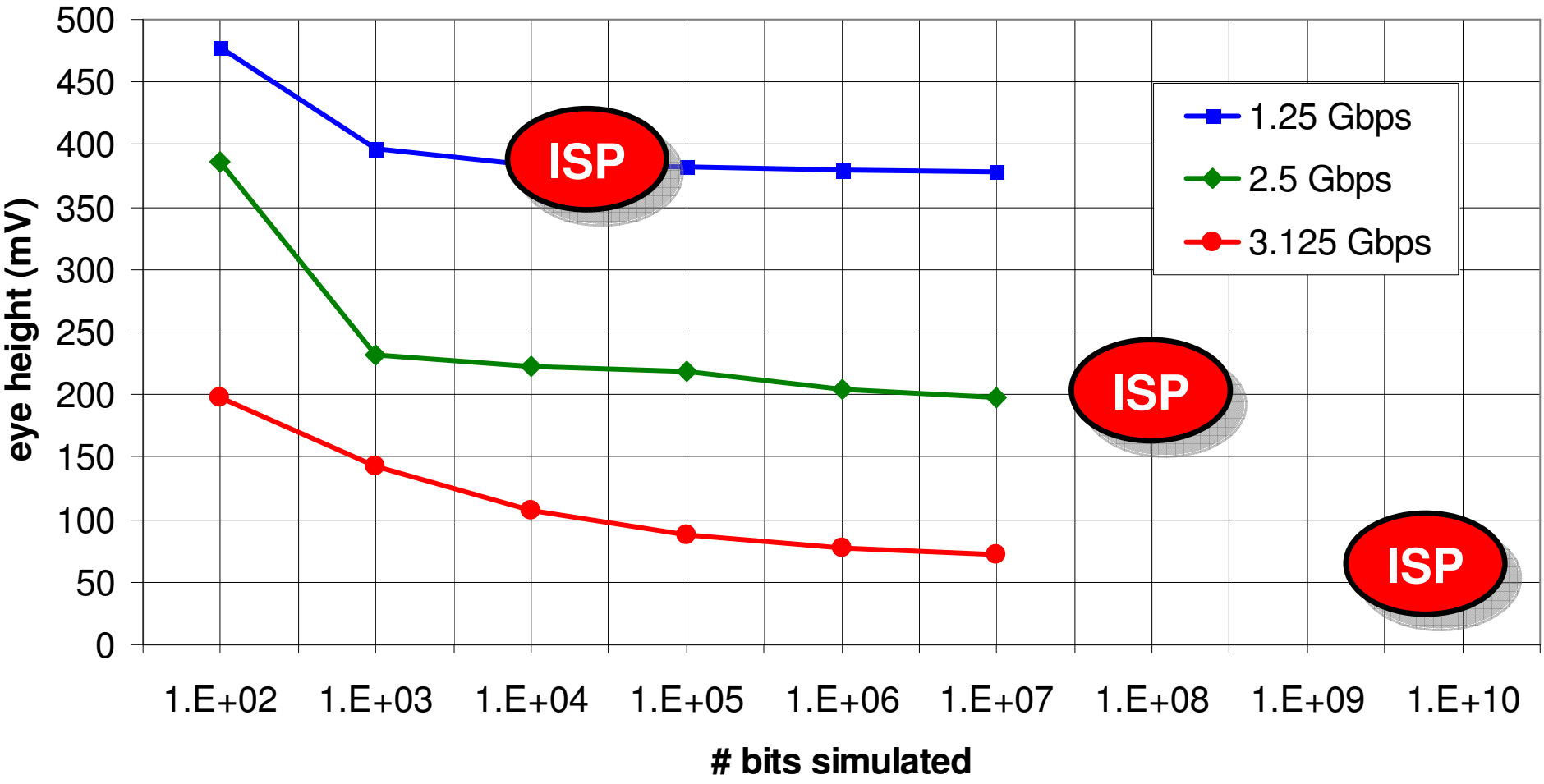
In which bit streams will the Test Pattern look the same?

24 Bits Confirms ISP Prediction



40 = 30, so 30 > *Answer* > 20, finding convergence yields 24 consistently

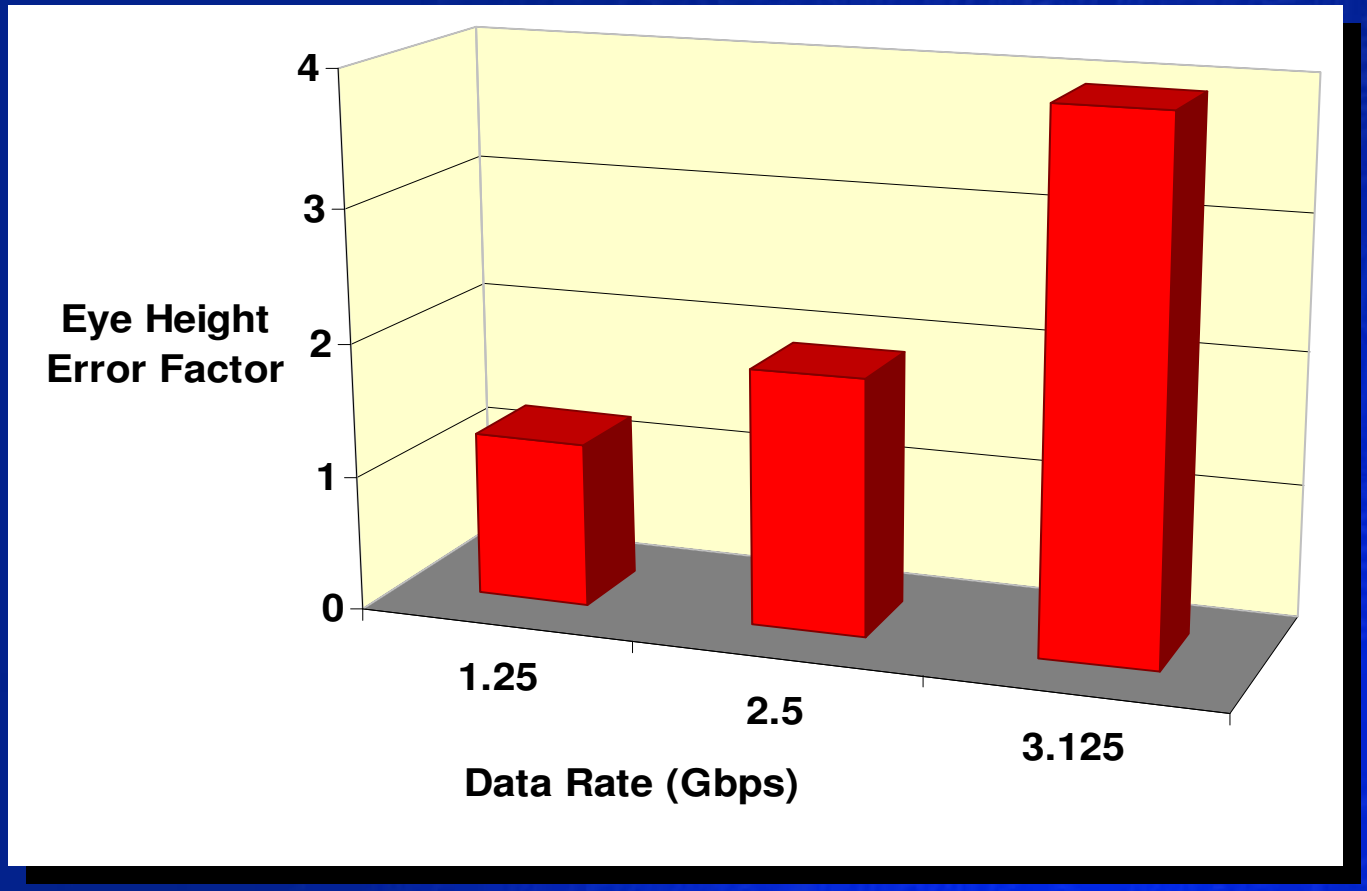
Eye Height vs Data Rate from CA



- Higher data rates take longer to converge
  - Eye height stabilizes at #bits(ISP)

Significant error if ISP not reached

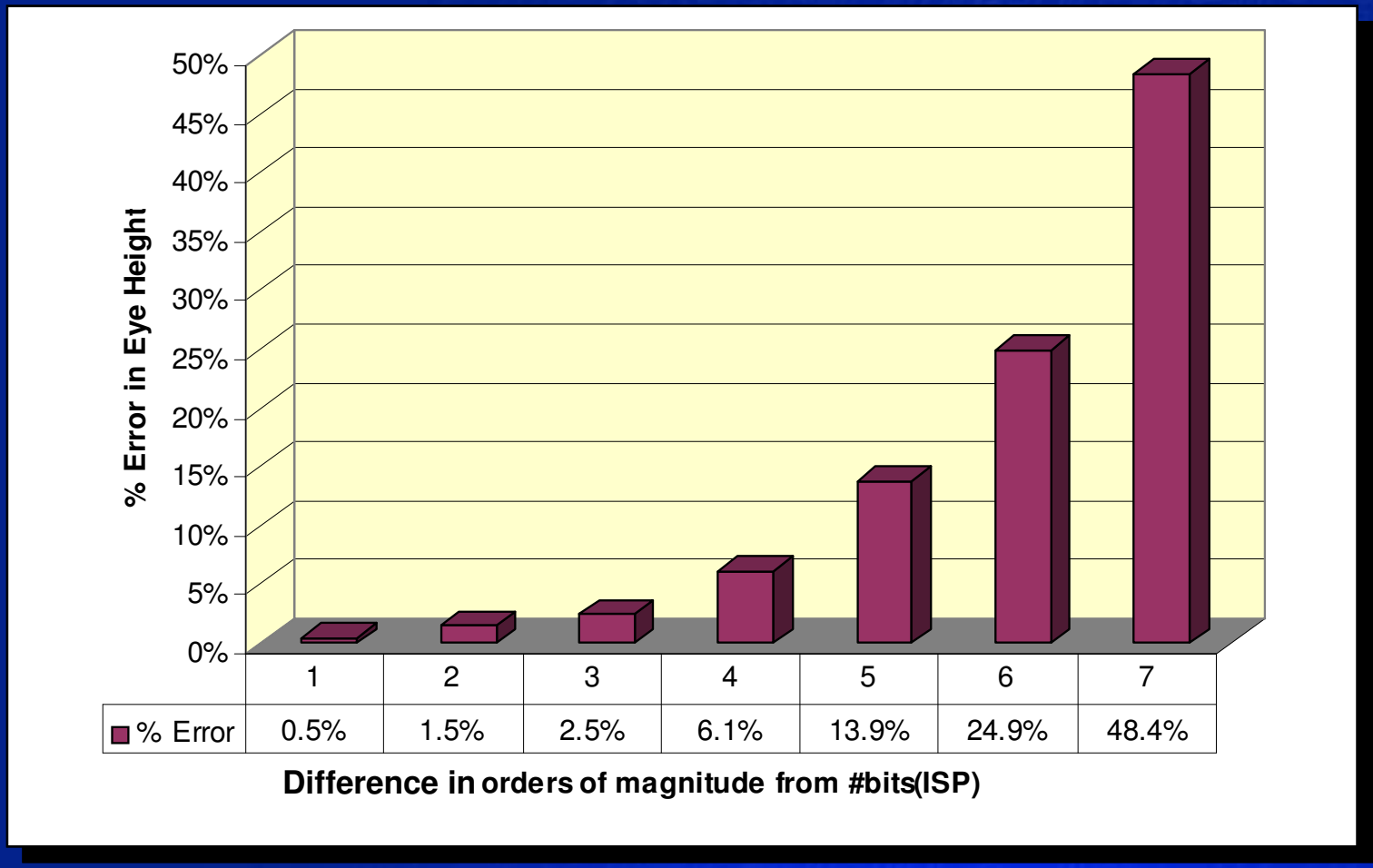
Eye Height Error for 100 bits vs ISP



- At 2.5 Gbps eye height at 100 bits is almost 2x wider than eye at ISP
  - Error factor grows exponentially with increasing data rate

Methodology is imperative at higher frequencies

But must we simulate to ISP?



At 2.5 Gbps, eye height error is less than 3% within 3 orders of magnitude of #bits(ISP)

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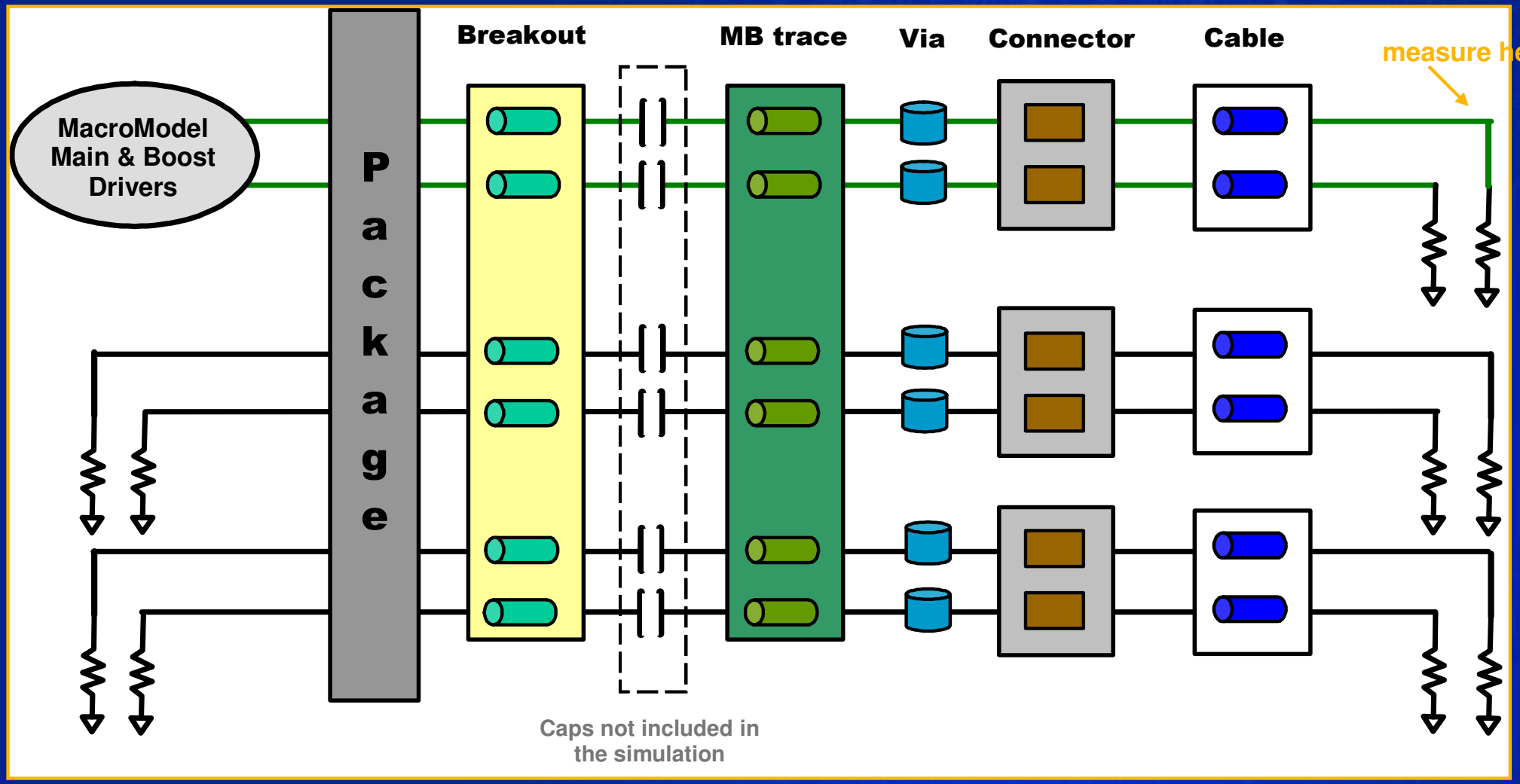
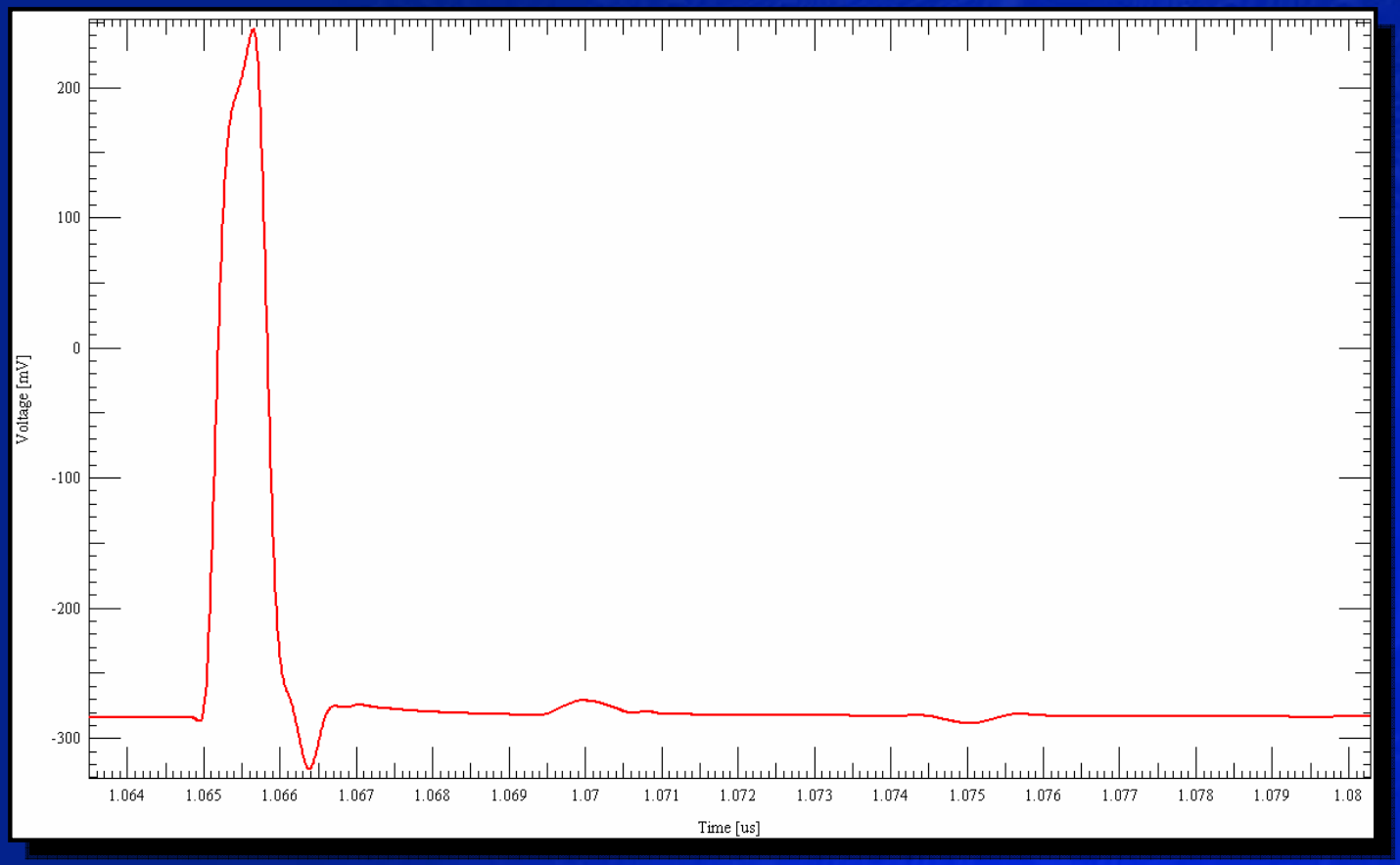
Serial-ATA Simulation Topology



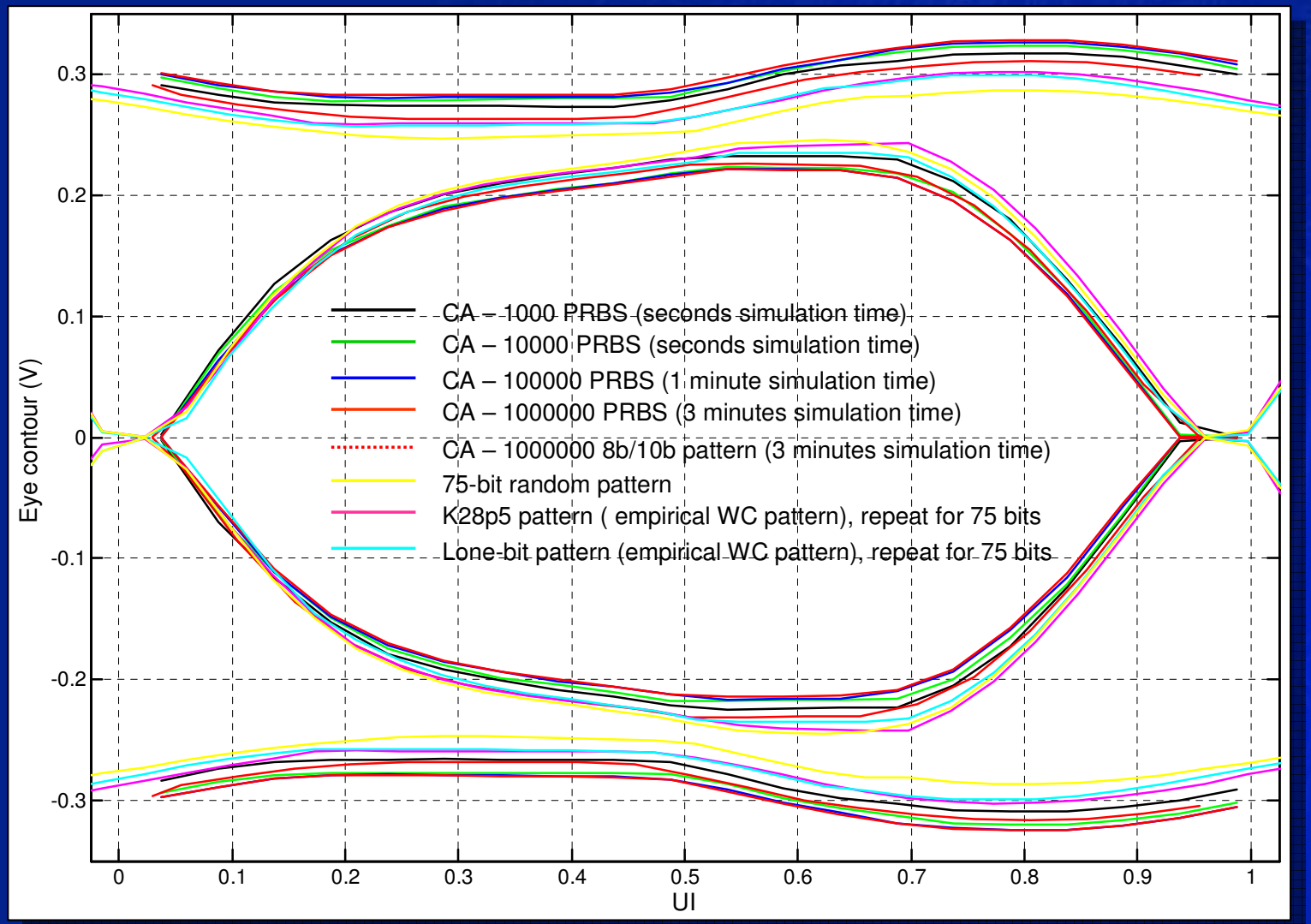
3 differential pairs organized per spec; Gen I - 1.5 Gbps, Gen II - 3.0 Gbps

ISP Sim Shows Clean Channel



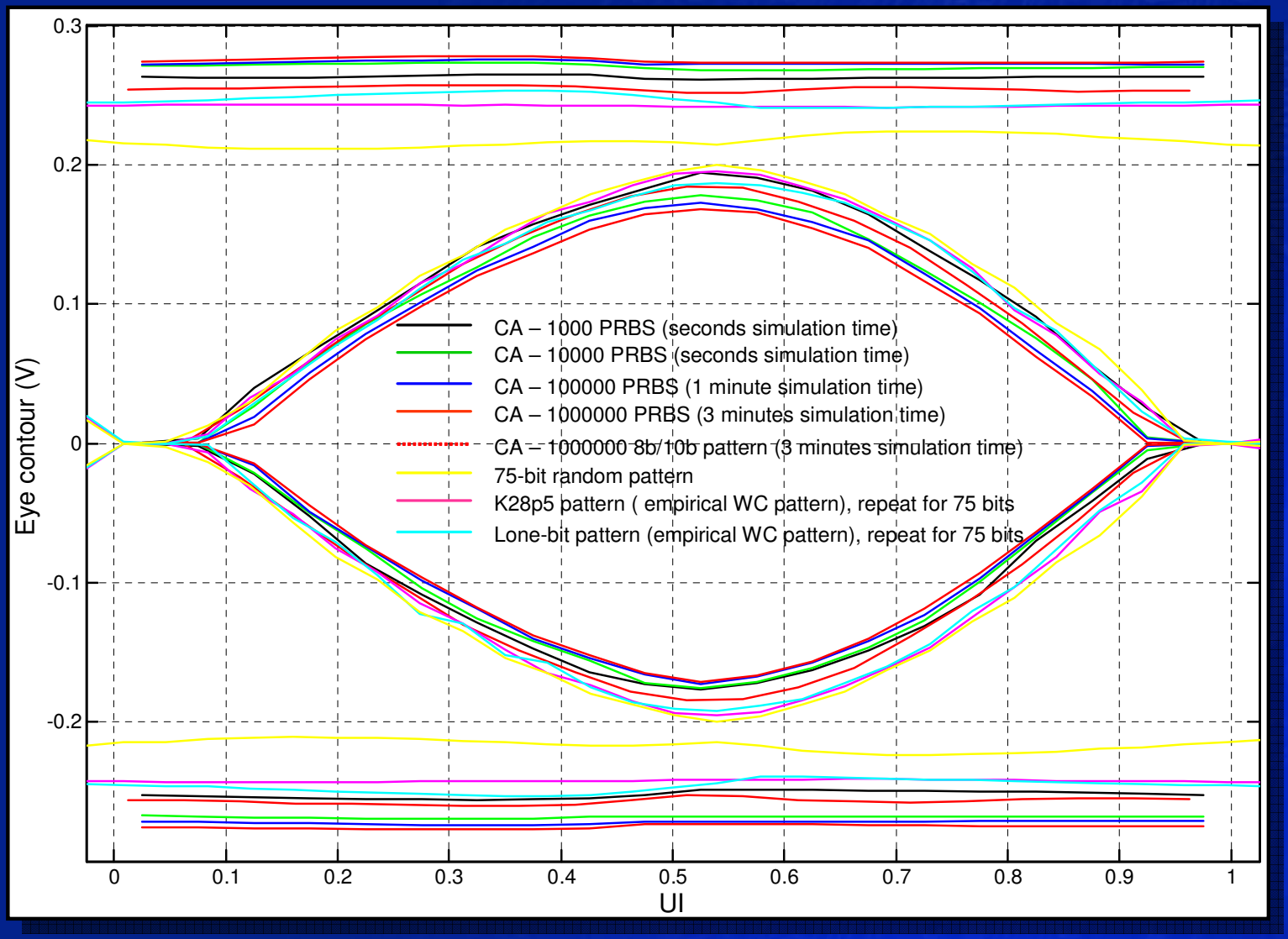
Is Channel Analysis important on a channel like this?

Eye Contour Generated from CA and HSpice Simulations (@1.5 Gbps)



CA long PRBS simulations predict worse eye openings than short empirical WC pattern simulations

Eye Contour Generated from CA and HSpice Simulations (@3.0 Gbps)



Higher frequency shows even greater difference between CA and empirical WC pattern simulations

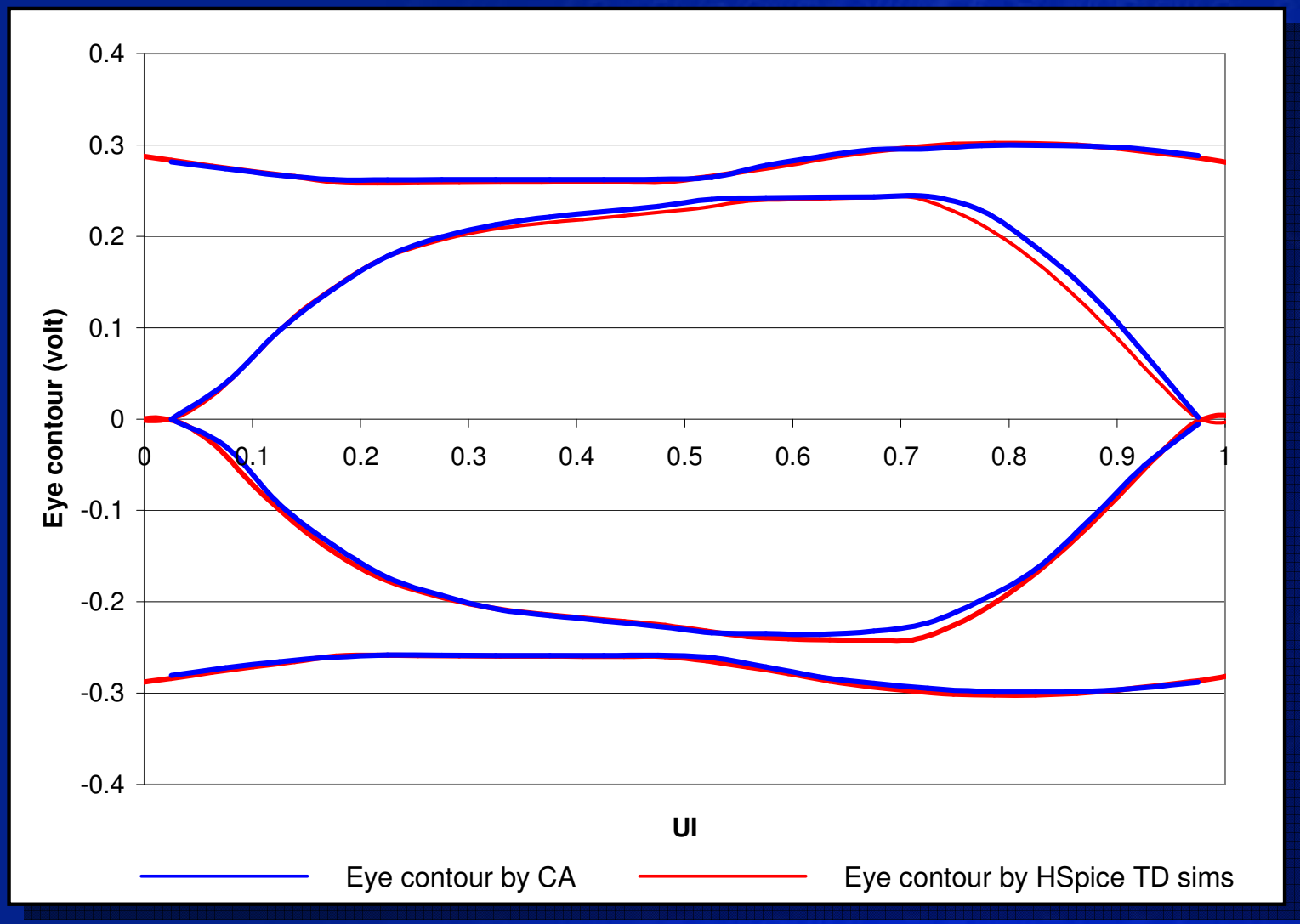
Quantitative Difference: CA vs HSpice TD

Data Rate	Tool	Stimulus Pattern	Worst Case Inside Eye Height	Worst Case Outside Eye Height
1.5 Gbps		1000-bit PRBS	428	627
			412	644
			408	650
			406	652
			427	627
		its)	437	604
		its)	433	599
		its)	443	574
3.0 Gbps	CA	1000-bit PRBS	320	521
		10000-bit PRBS	305	543
		100000-bit PRBS	298	550
		1000000-bit PRBS	290	556
		1000000-bit 8b/10b	319	517
	HSpice	K28p5 (repeat for 75 bits)	336	486
		Lone-bit (repeat for 75 bits)	325	506
		Random (repeat for 75 bits)	340	448

Fewer bits causes inside eye inaccuracy of 50mV and outside eye over 100 mV

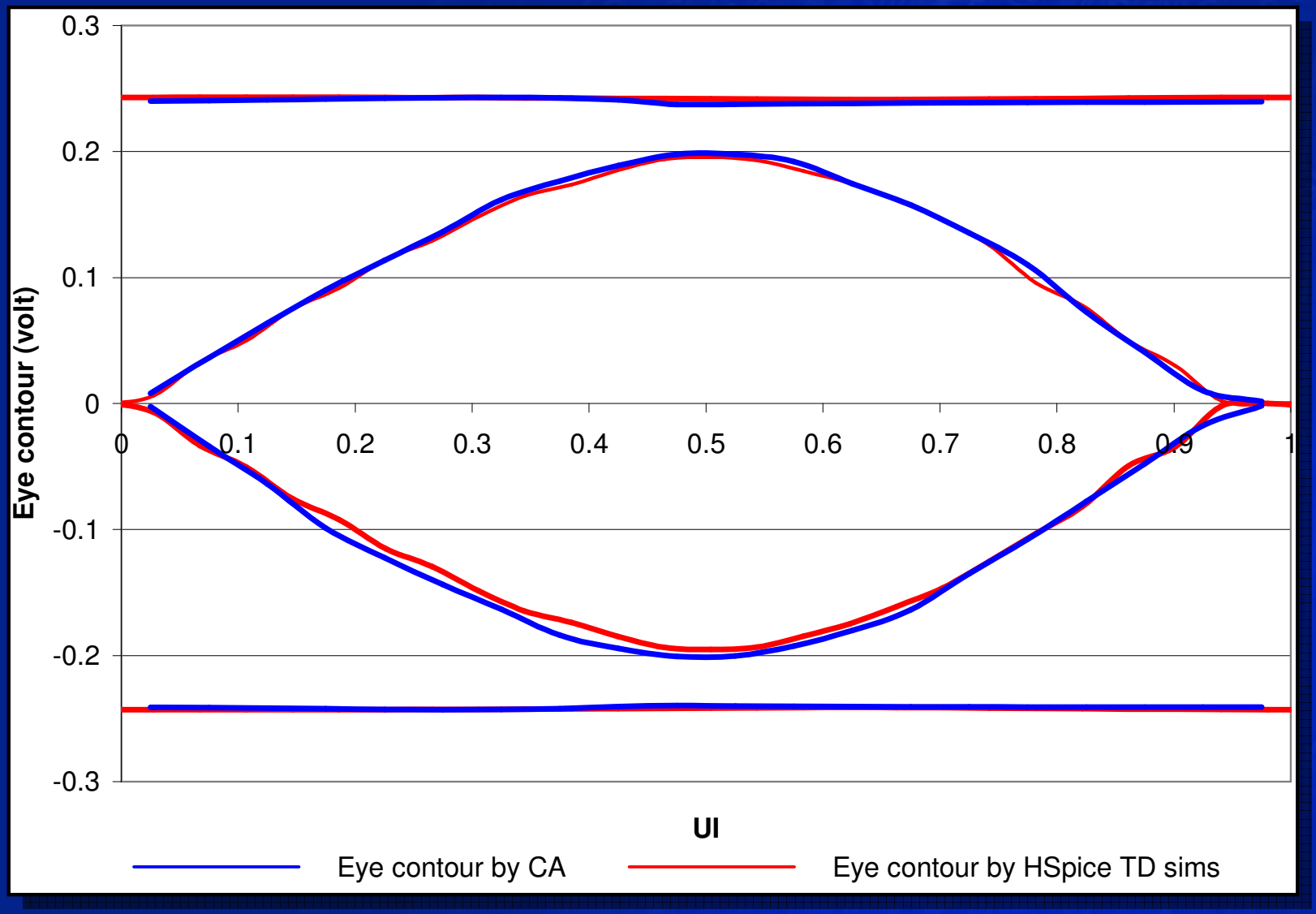
This quantifies the difference between two methodologies on S-ATA. However, do the tools correlate given the same input pattern?

Eye Correlation using CA and HSpice with same stimulus pattern (@1.5 Gbps)



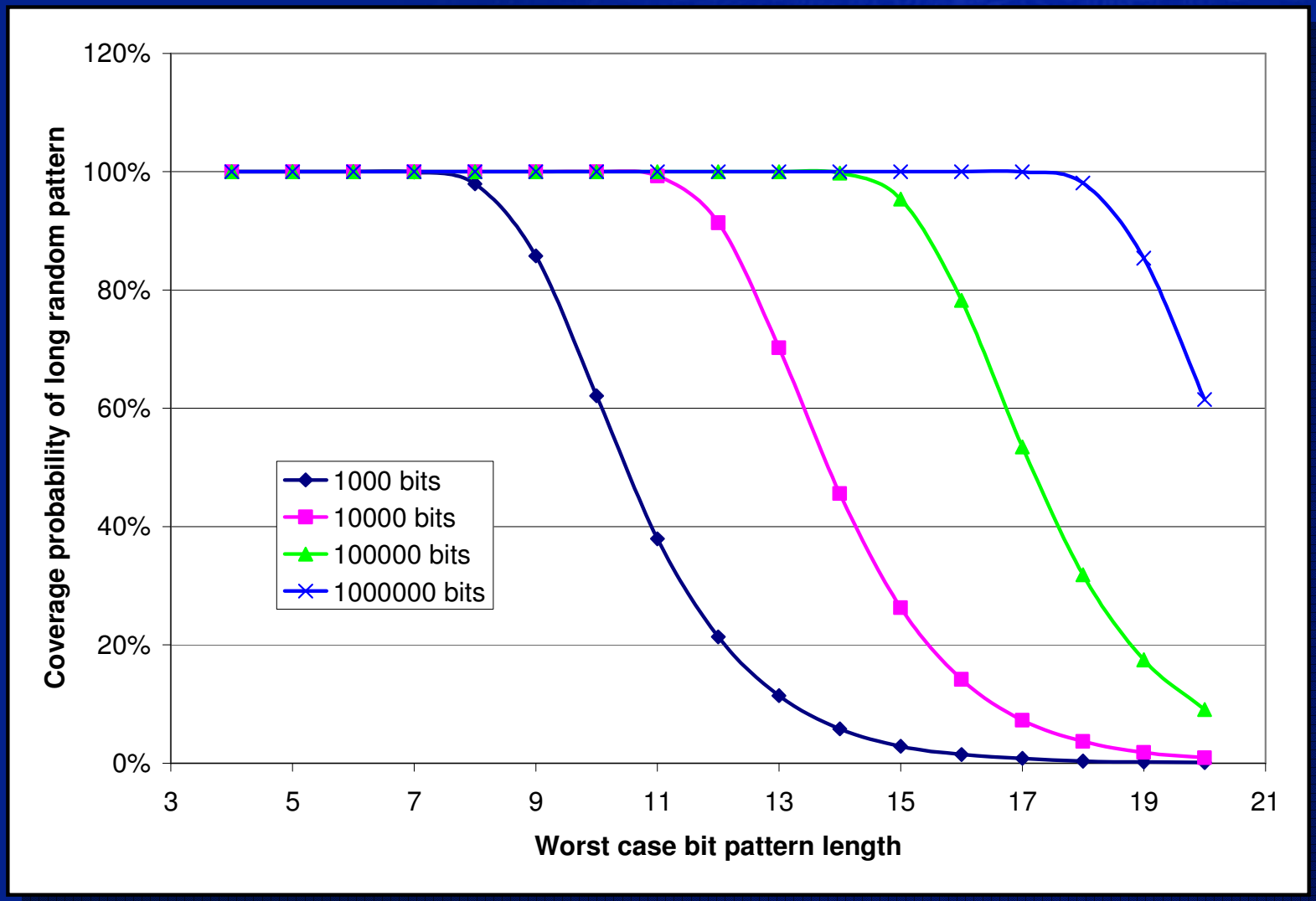
Correlation based on 75-bit input pattern

Eye Correlation using CA and HSpice with same stimulus pattern (@3 Gbps)



Correlation based on 150-bit input pattern

Probability of Long Random Pattern Covering Worst-case Patterns



If WC pattern length <= 18 bits, the probability for a 1M bit PRBS pattern covering the WC pattern is 98.1%

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Summary & Conclusions

- Introduced new methodologies and tools
  - illustrated using PCI Express & S-ATA
- Quantifying an ISP provides guidance on how to derive a meaningful eye diagram
- The speed of Channel Analysis allows more thorough pre-hardware link characterization
  - improved results by 20% to 260% in cases shown
- Some correlation shown, more in Resources
- Many new discoveries still to come

Resources

- 11 items in Reference Materials section in paper
- Channel Analysis and MGH tools demo at Cadence booth
- 3 Agilent/Cadence CA correlation papers now available online at www.allegrosi.com
- Additional technical detail at
  - http://www.allegrosi.com/optimize/AdvancedTechniques/MGH.asp

Thank You

Feel free to contact us for more info